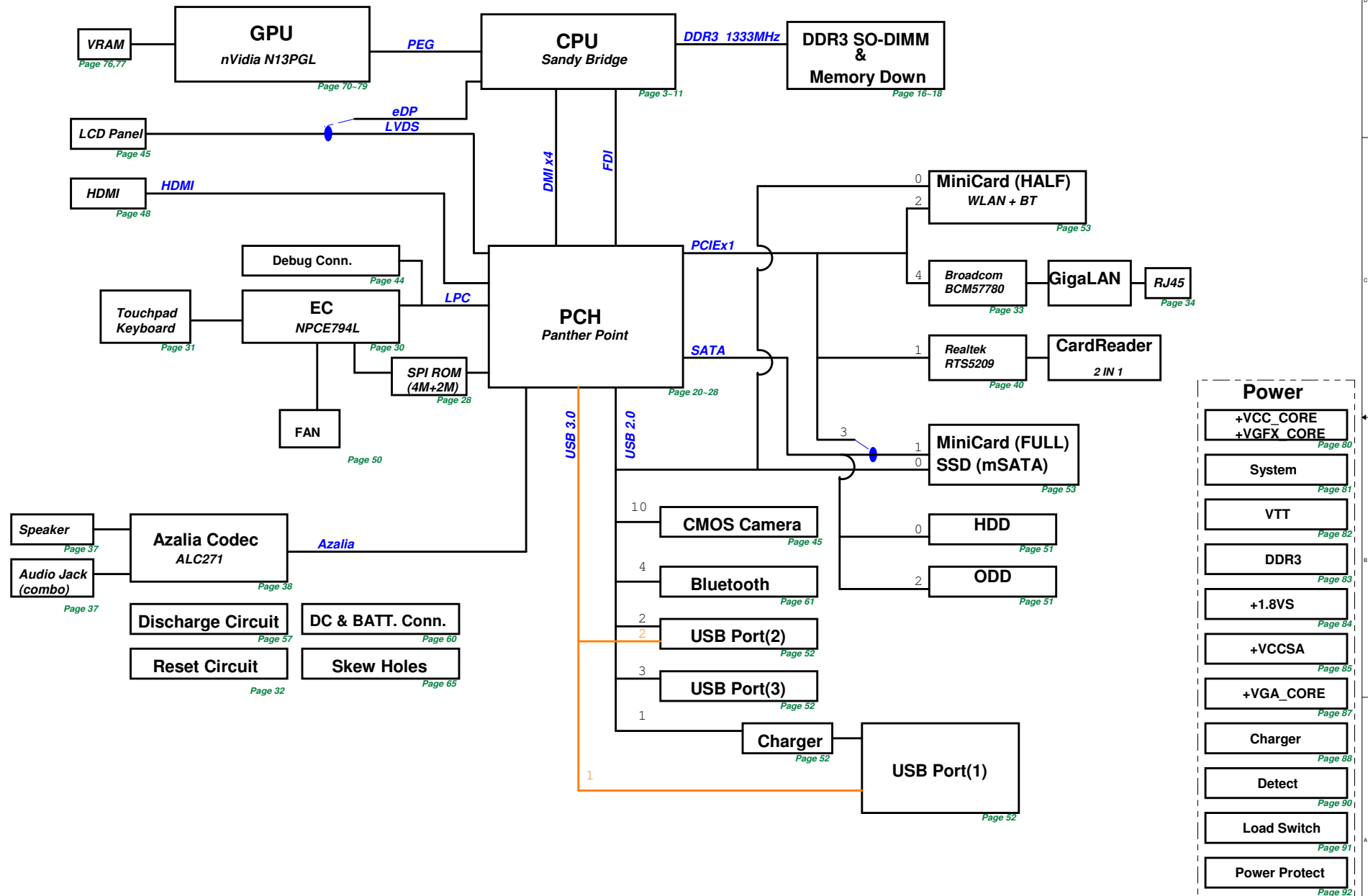


MA50 Ultrabook Block Diagram Rev 1.0



PCH_CPT
GPIO

PCH_CPT GPIO	Use As	Signal Name	Internal & External Pull-up/down	Power
GPIO 00				
GPIO 01				
GPIO [2:5]				
GPIO 06				
GPIO 07				
GPIO 08				
GPIO 09				
GPIO 10				
GPIO 11				
GPIO 12				
GPIO 13				
GPIO 14				
GPIO 15				
GPIO 16				
GPIO 17				
GPIO 18				
GPIO 19				
GPIO 20				
GPIO 21				
GPIO 22				
GPIO 23				
GPIO 24				
GPIO 25				
GPIO 26				
GPIO 27				
GPIO 28				
GPIO 29				
GPIO 30				
GPIO 31				
GPIO 32				
GPIO 33				
GPIO 34				
GPIO 35				
GPIO 36				
GPIO 37				
GPIO 38				
GPIO 39				
GPIO 40				
GPIO 41				
GPIO 42				
GPIO 43				
GPIO 44				
GPIO 45				
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GPIO 47				
GPIO 48				
GPIO 49				
GPIO 50				
GPIO 51				
GPIO 52				
GPIO 53				
GPIO 54				
GPIO 55				
GPIO 56				
GPIO 57				
GPIO 58				
GPIO 59				
GPIO 60				
GPIO 61				
GPIO 62				
GPIO 63				
GPIO 64				
GPIO 65				
GPIO 66				
GPIO 67				
GPIO 72				
GPIO 73				
GPIO 74				
GPIO 75				

WWW.AliSaler.Com

EC
NPCE795L

EC GPIO	Use As	Signal Name
GPA0		
GPA1		
GPA2		
GPA3		
GPA4		
GPA5		
GPA6		
GPA7		
GPB0		
GPB1		
GPB2		
GPB3		
GPB4		
GPB5		
GPB6		
GPB7		
GPC0		
GPC1		
GPC2		
GPC3		
GPC4		
GPC5		
GPC6		
GPC7		
GPD0		
GPD1		
GPD2		
GPD3		
GPD4		
GPD5		
GPD6		
GPD7		
GPE0		
GPE1		
GPE2		
GPE3		
GPE4		
GPE5		
GPE6		
GPE7		
GPF0		
GPF1		
GPF2		
GPF3		
GPF4		
GPF5		
GPF6		
GPF7		
PGP0		
PGP1		
PGP2		
PGP6		
GPH0		
GPH1		
GPH2		
GPH3		
GPH4		
GPH5		
GPH6		
GPI0		
GPI1		
GPI2		
GPI3		
GPI4		
GPI5		
GPI6		
GPI7		
GPJ0		
GPJ1		
GPJ2		
GPJ3		
GPJ4		
GPJ5		

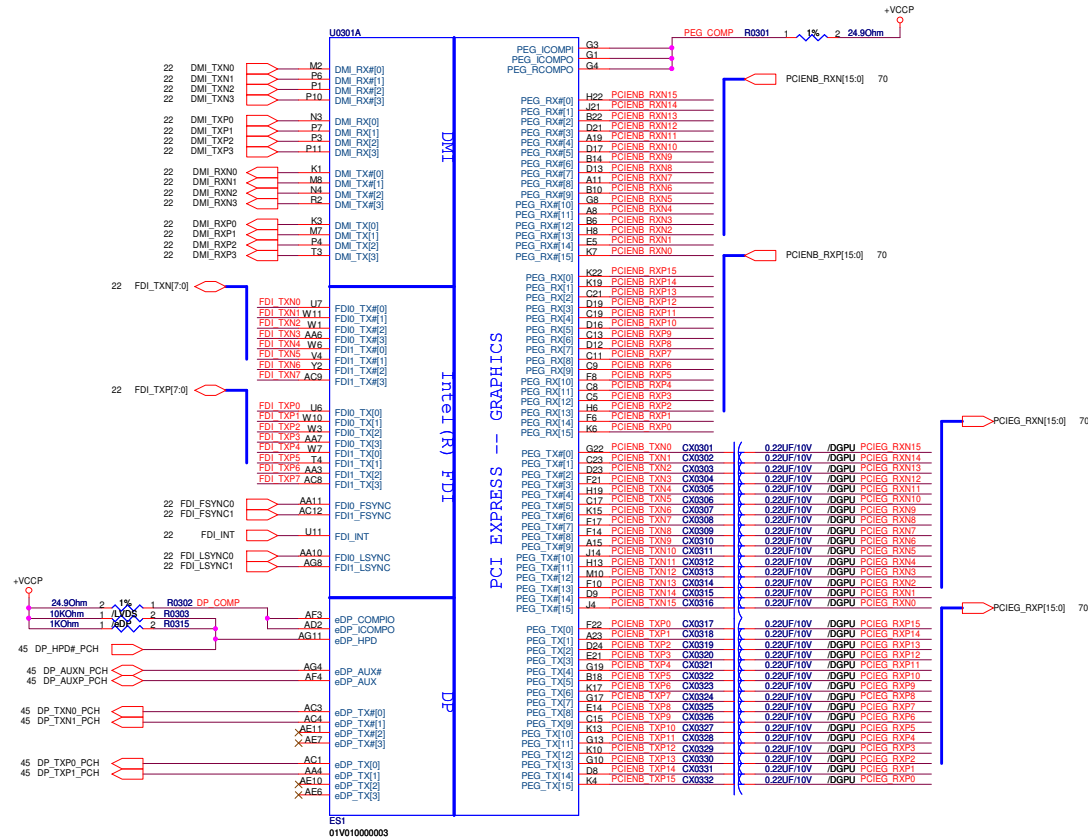
SM_BUS ADDRESS :

SM-Bus Device	SM-Bus Address
SO-DIMM 0	1010000x (A0h)
SO-DIMM 1	1010001x (A4h)

PCIE 1	N/A
PCIE 2	Minicard WLAN
PCIE 3	N/A
PCIE 4	USB3.0
PCIE 5	N/A
PCIE 6	GLAN
PCIE 7	N/A
PCIE 8	N/A

SATA0	SATA HDD
SATA1	N/A
SATA2	SATA ODD
SATA3	N/A
SATA4	N/A
SATA5	N/A

USB 0	USB Port (1)
USB 1	USB Port (2)
USB 2	USB 3.0 Port (3)
USB 3	USB Port (4)
USB 4	N/A
USB 5	N/A
USB 6	N/A
USB 7	N/A
USB 8	CMOS Camera
USB 9	WLAN
USB 10	Card Reader
USB 11	N/A
USB 12	N/A
USB 13	N/A

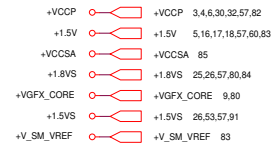
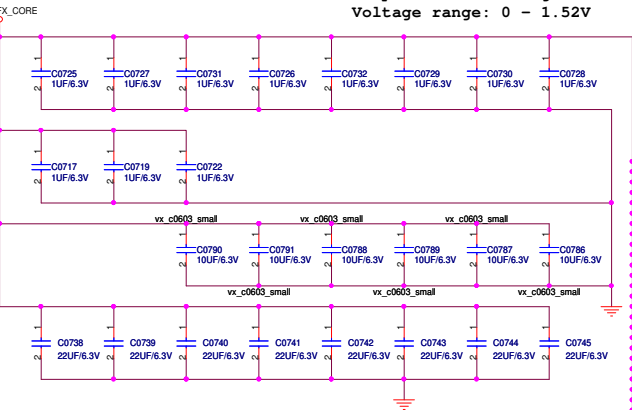


Decoupling guide from Intel PDDG R0.8

+VGFX_CORE
1uF * 11pcs
10uF * 6pcs
22uF * 6pcs

+VGFX_CORE
1uF * 11pcs
10uF * 6pcs
22uF * 8pcs(power request)

Graphics core voltage
Voltage range: 0 - 1.52V



U0301G

AA46 VAXG21
AB47 VAXG20
AB50 VAXG19
AB51 VAXG18
AB52 VAXG17
AB53 VAXG16
AB55 VAXG15
AB56 VAXG14
AB58 VAXG13
AB59 VAXG12
AC61 VAXG11
AD47 VAXG10
AD48 VAXG9
AD50 VAXG8
AD51 VAXG7
AD52 VAXG6
AD53 VAXG5
AD55 VAXG4
AD56 VAXG3
AD58 VAXG2
VAXG1
AE46 VAXG0
NA45 VAXG55
PA7 VAXG54
PA8 VAXG53
P50 VAXG52
P51 VAXG51
P52 VAXG50
P53 VAXG49
P55 VAXG48
P56 VAXG47
P61 VAXG46
T48 VAXG45
T58 VAXG44
T59 VAXG43
U46 VAXG42
U47 VAXG41
U48 VAXG40
V48 VAXG39
V50 VAXG38
V51 VAXG37
V52 VAXG36
V53 VAXG35
V55 VAXG34
V56 VAXG33
V58 VAXG32
V59 VAXG31
W50 VAXG30
W51 VAXG29
W52 VAXG28
W53 VAXG27
W55 VAXG26
W56 VAXG25
W61 VAXG24
Y48 VAXG23
Y61 VAXG22

POWER

GRAPHICS

DDR3 - 1.5V RAILS

SM_VREF

DDR3 Reference Voltage

+1.5VS_VCCDDQ

R1.1
add S3 power reduction

+V_SM_VREF 10mV

+V_SM_VREF

AY43 -V SM_VREF

R0703 1K0hm

R0710 1K0hm

C0794 0.1uF/10V

MAX: 5A

C0704 1uF/6.3V

C0709 1uF/6.3V

C0705 1uF/6.3V

C0706 1uF/6.3V

C0707 1uF/6.3V

C0708 1uF/6.3V

C0713 1uF/6.3V

C0710 1uF/6.3V

C0712 1uF/6.3V

C0711 1uF/6.3V

C0704 1uF/6.3V

C0709 1uF/6.3V

C0705 1uF/6.3V

C0706 1uF/6.3V

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C0708 1uF/6.3V

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C0711 1uF/6.3V

C0704 1uF/6.3V

C0709 1uF/6.3V

C0705 1uF/6.3V

C0706 1uF/6.3V

C0707 1uF/6.3V

C0708 1uF/6.3V

C0713 1uF/6.3V

C0710 1uF/6.3V

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C0711 1uF/6.3V

C0704 1uF/6.3V

C0709 1uF/6.3V

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C0706 1uF/6.3V

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C0708 1uF/6.3V

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C0704 1uF/6.3V

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C0711 1uF/6.3V

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C0708 1uF/6.3V

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C0712 1uF/6.3V

C0711 1uF/6.3V

C0704 1uF/6.3V

C0709 1uF/6.3V

C0705 1uF/6.3V

C0706 1uF/6.3V

C0707 1uF/6.3V

C0708 1uF/6.3V

C0713 1uF/6.3V

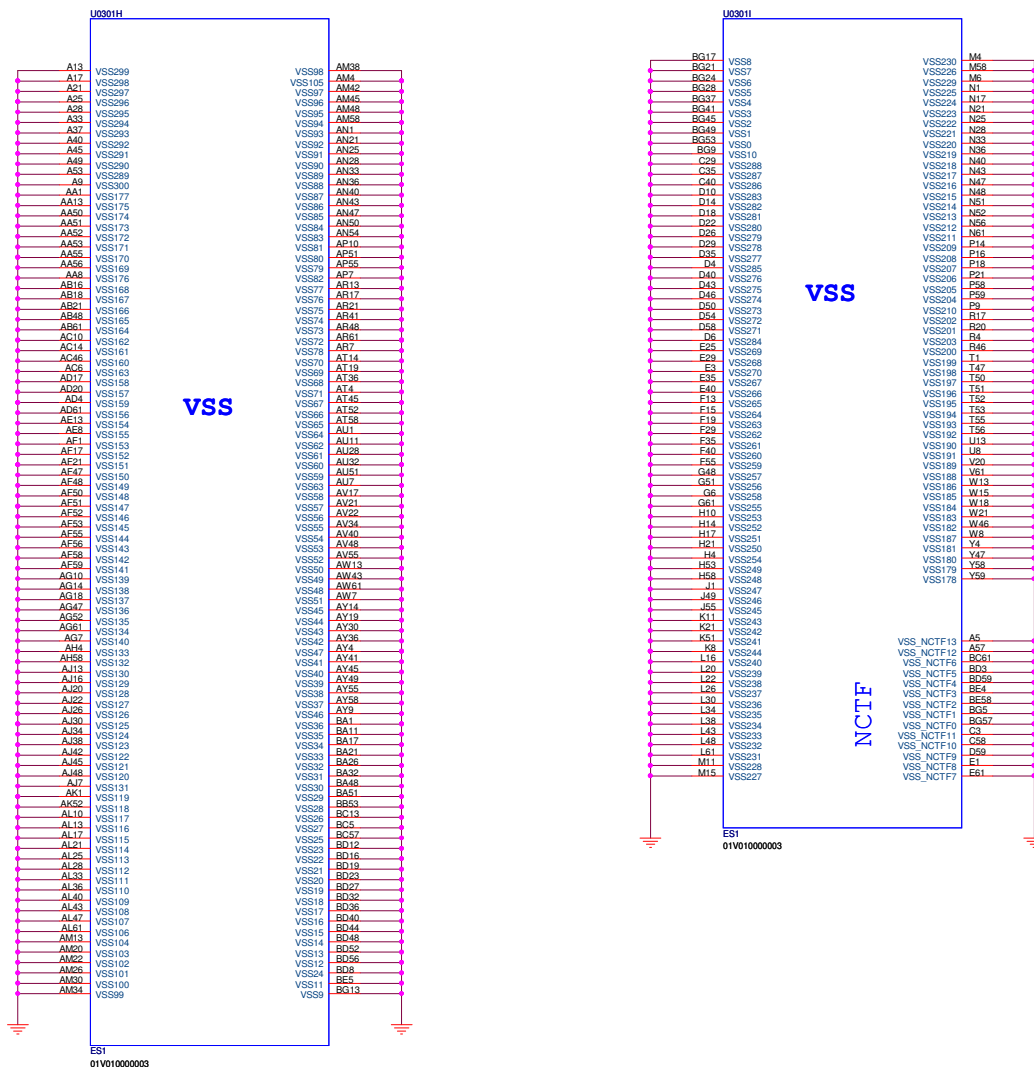
C0710 1uF/6.3V

C0712 1uF/6.3V

C0711 1uF/6.3V

C0704 1uF/6.3V

C0709 1uF/6.3V



CFG strapping information:

CFG[2]: PCIE Static Numbering Lane Reversal- CFG[2] is for the 16x

- 1: (Default) Normal Operation, Lane # definition matches socket pin map definition
- 0: Lane Numbers Reversed

CFG[4]: Embedded DisplayPort Detection

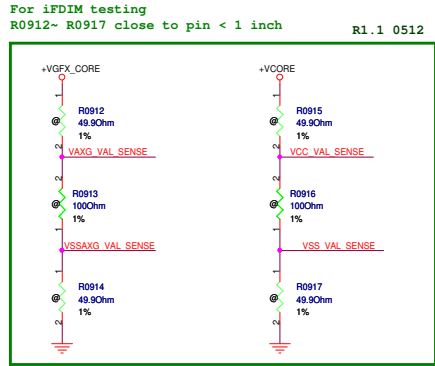
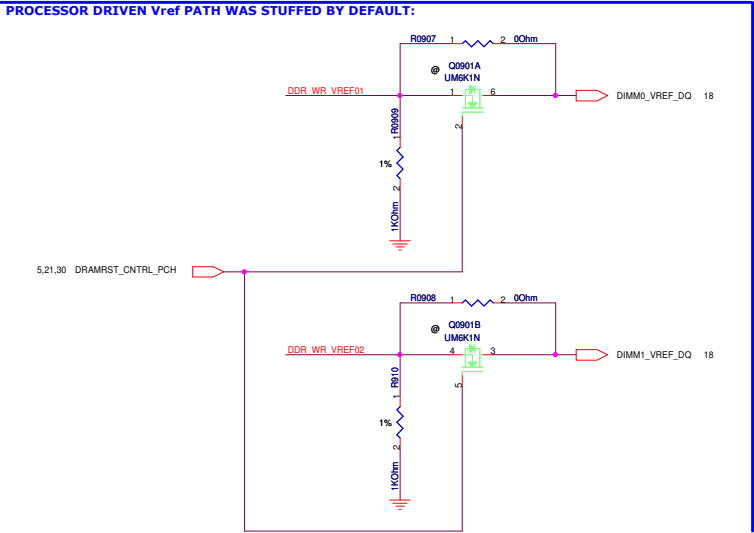
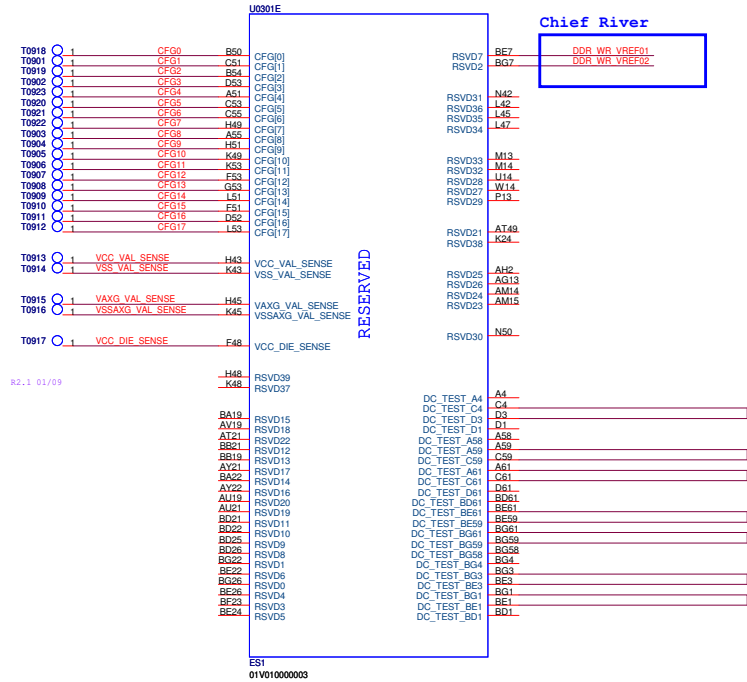
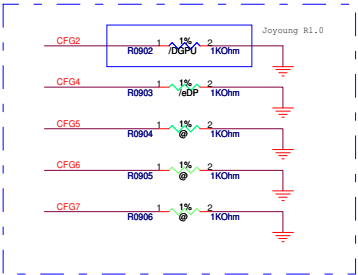
- 1: (Default) Disabled ; No Physical Display Port attached to Embedded DisplayPort
- 0: Enabled ; An external Display Port device is connected to the Embedded Display Port

CFG[6:5]: PCI Express Port Bifurcation Straps

- 11 : (Default) x 1 6
- 10 : x 8 , x 8
- 01 : Reserved
- 00 : x 8 , x 4 , x 4

CFG[7]: PEG DEFER TRAINING

- 1: (Default) PEG Train immediately following xxRESETB de assertion
- 0: PEG Wait for BIOS training



CPU XDP connector

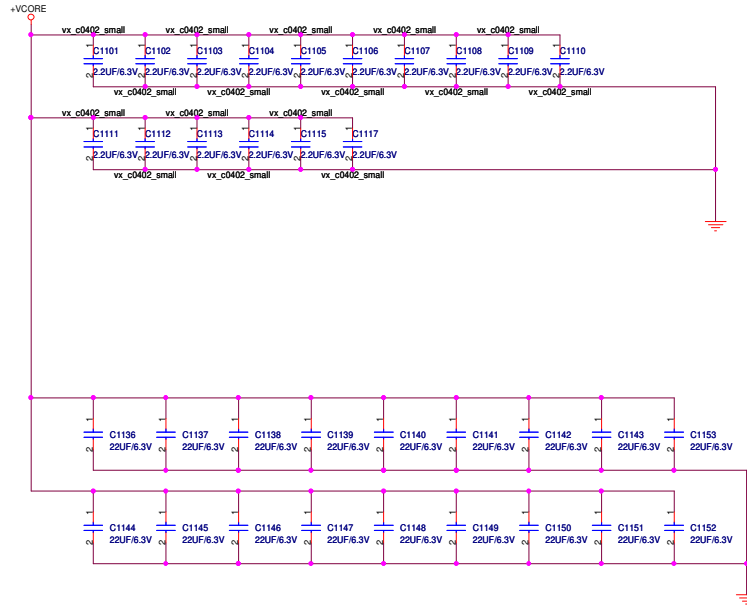
Check Connector

PCH XDP connector

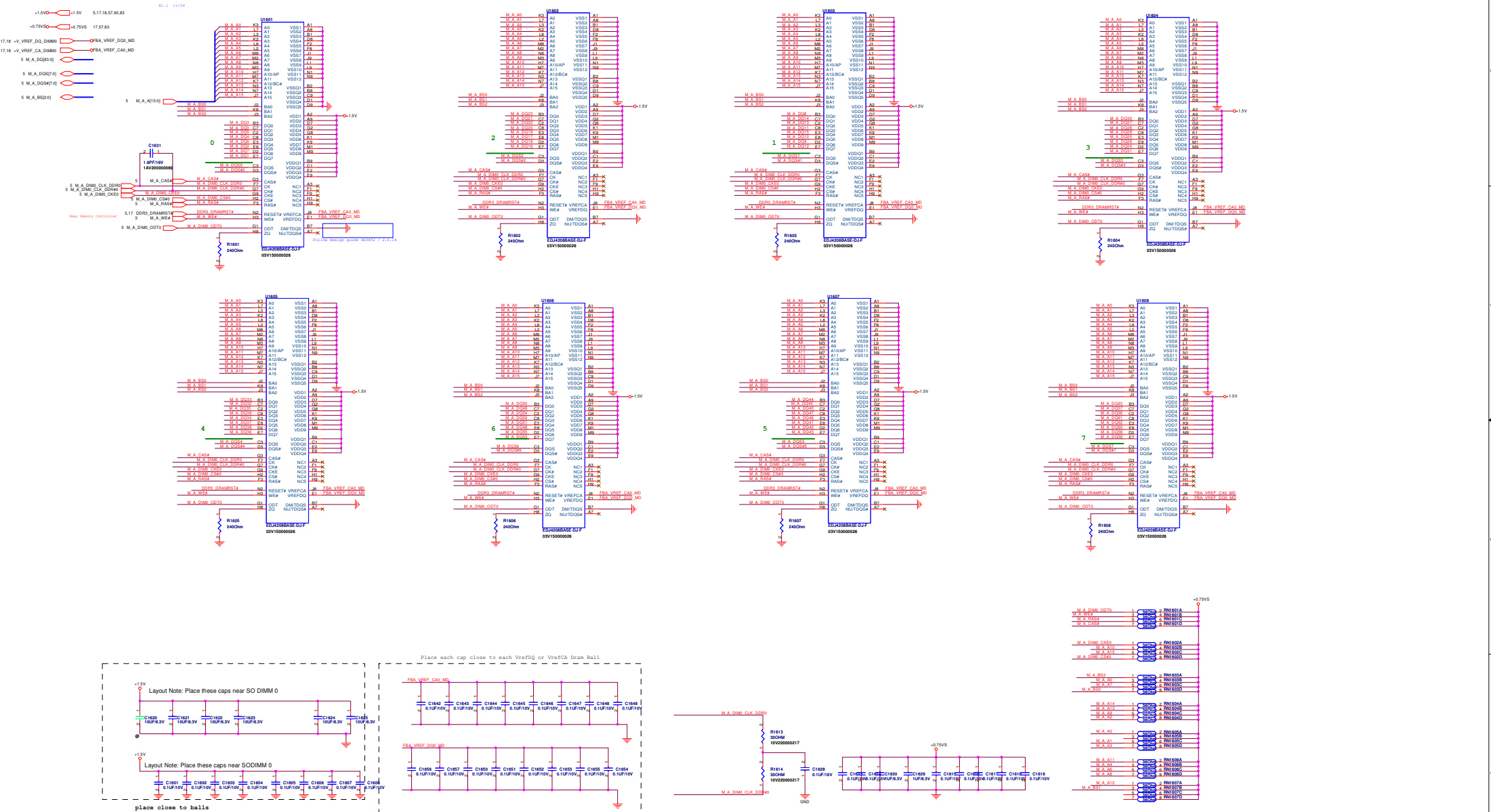
PEGATRON		Title : CPU_PCH_XDP	
BG1-HW RD Div.2-NB RD Dept.5		Engineer: Joyoung_Chianhg	
Size	Project Name		Rev
Custom	MA50		1.0
Date: Monday, February 13, 2012		Sheet	10 of 93

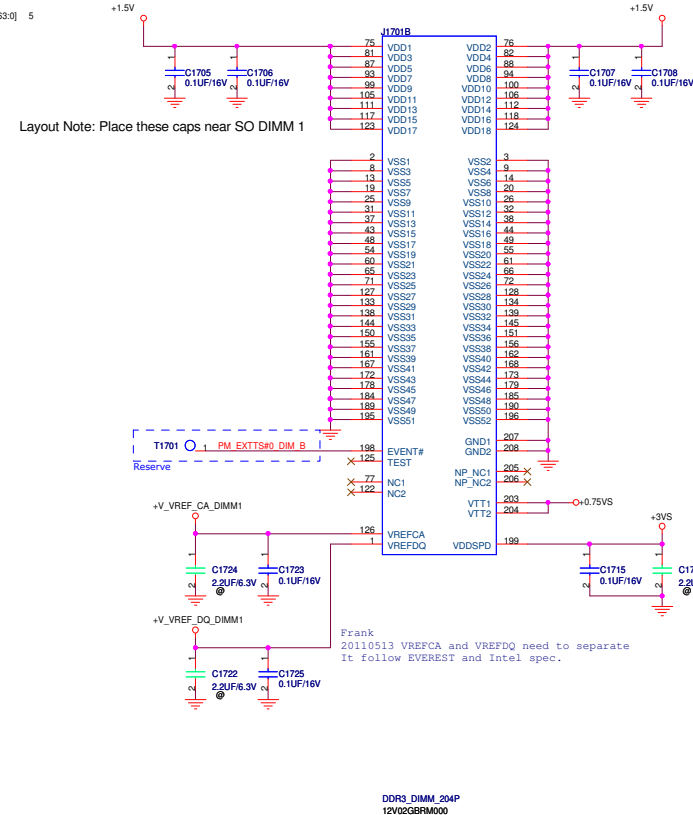
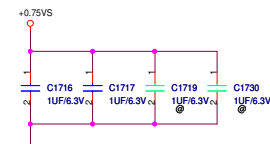
Chief River
Decoupling guide from Intel PDDG R0.8
+VCORE 2.2uF * 16 pcs
22uF * 12 pcs

Chief River
+VCORE 2.2uF * 16 pcs
22uF * 18 pcs (power request)



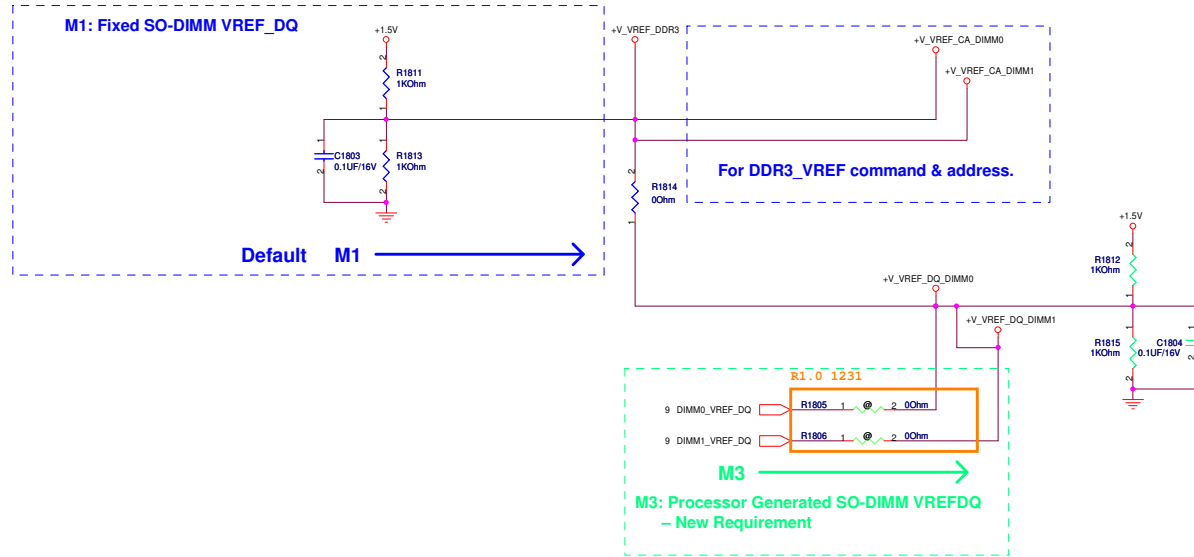
Memory Down CH A





PEGATRON		Title : DDR3(2)_SO-DIMM1
PEGATRON COMPUTER INC		Engineer: Jyoung_Chianhg
Size C	Project Name MA50	Rev 1.0
Date: Monday, February 13, 2012		Sheet 17 of 93

DDR3 Vref

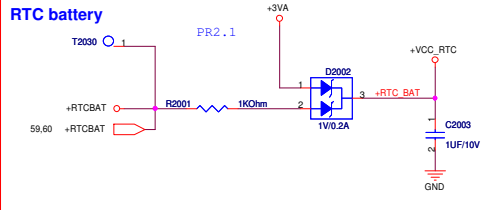


If support M3 :
 1. Mount R1802,R1803,R1805,R1806,R1810,R1811,C1802
 2. Un mount R1801,R1804

+1.5V 5,16,17,57,60,83
 +V_VREF_CA_DIMM0 16,17
 +V_VREF_DQ_DIMM0 16,17

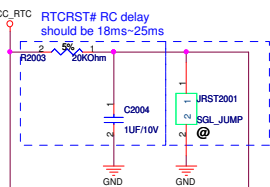
+3V 24,45,57,59,61,91
 +5VSUS 51,57,59,91
 +5VA 37,60,81,91

RTC battery



Request by CSC
for CMOS clear
function

CMOS Settings	JRST2001
Clear CMOS	Shunt
Keep CMOS	Open (Default)



INTVRMEN: Integrated SUS 1.05V VRM Enables
Low: Enable External VRs
High: Enable Internal VRs



TPM Settings	JRST2002
Clear ME RTC Registers	Shunt
Keep ME RTC Registers	Open (Default)

Intel I:5 Design Guide, page 260

isolate schematic for ACZ_SYNC and SDOUT follow EIH31

R1.0
For JTAG to pull high and low.

Remove JTAG schematic

Strap information:

SB_SPKR: No reboot strap
Low: Disable (Default)
High: Enable

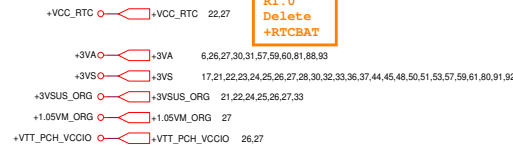
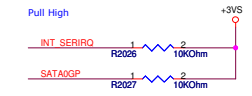
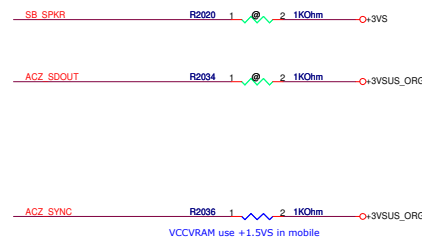
ACZ_SDOUT:

1. Flash descriptor security:
Sampled Low: in effect.
Sampled High: override

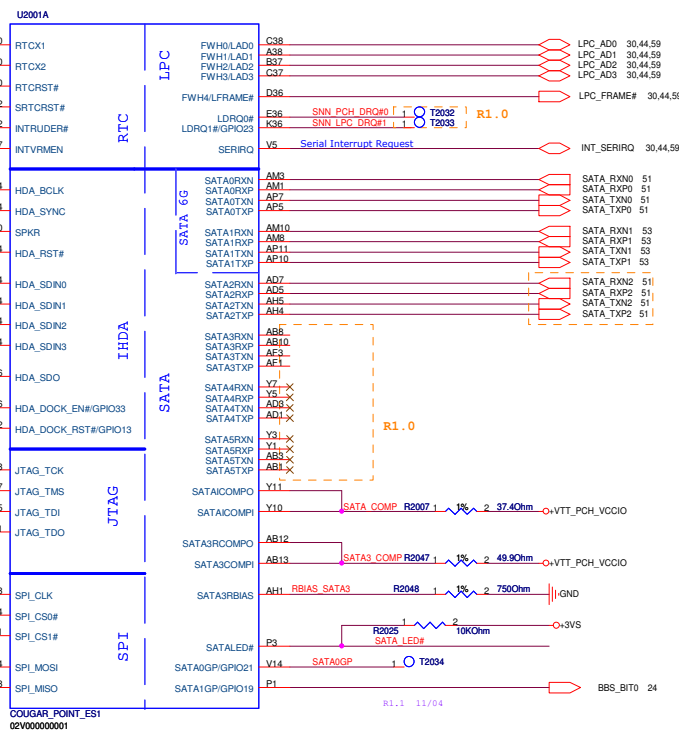
2. ACZ_SDOUT which sample high on the rising edge of PWROK
Will also disable Intel ME.

ACZ_SYNC: On Die PLL VR voltage selector

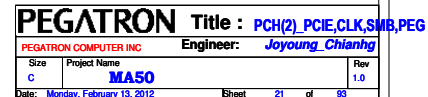
Low: 1.8V (Default)
High: 1.5V
note : CRB has no strap
Hiron River Platform Schematic Design Checklist
(438390 page 48)

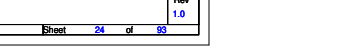
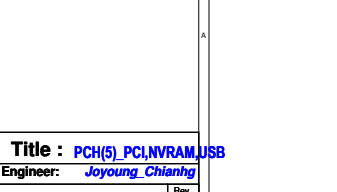
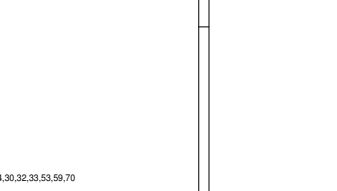
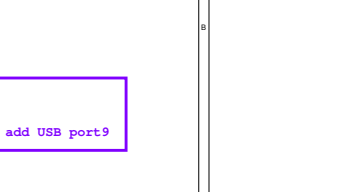
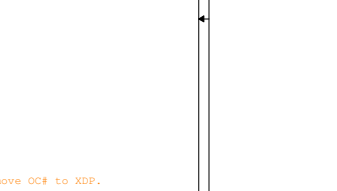
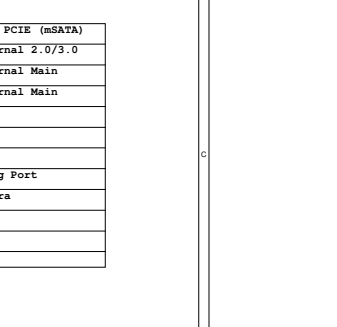
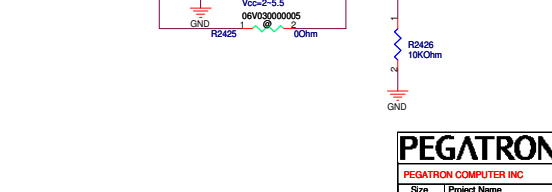
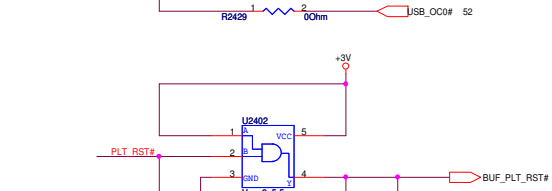
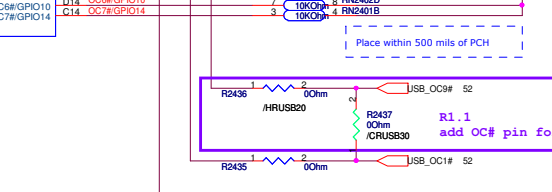
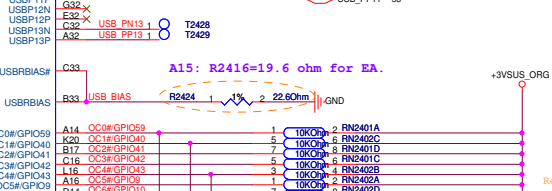
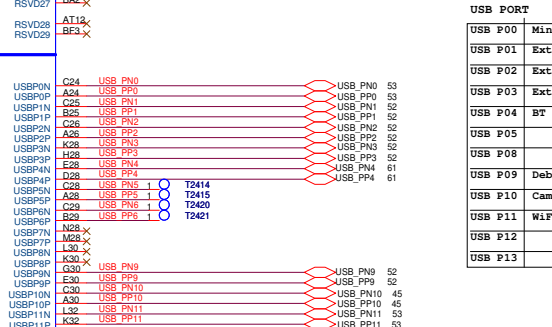
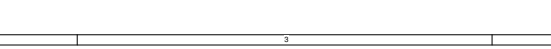
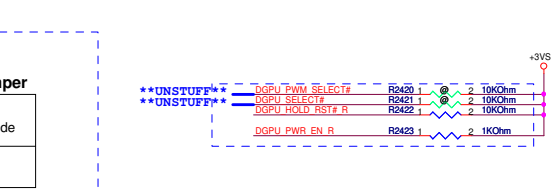
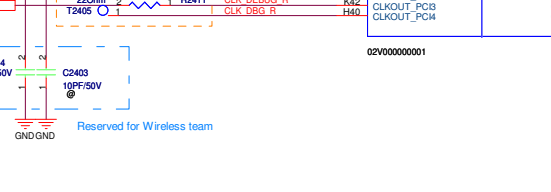
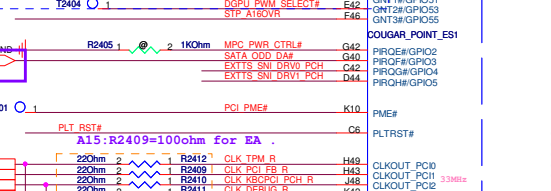
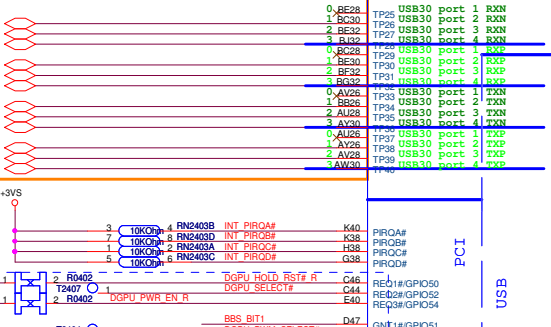
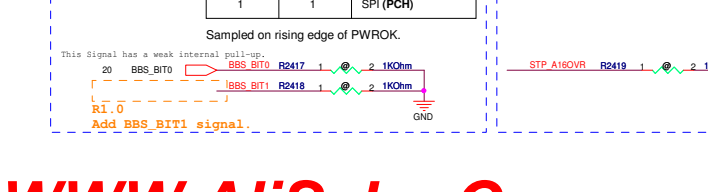
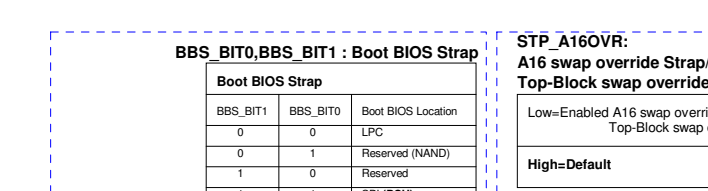
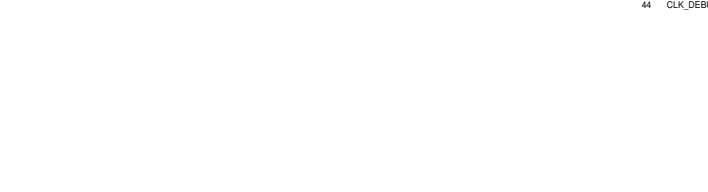
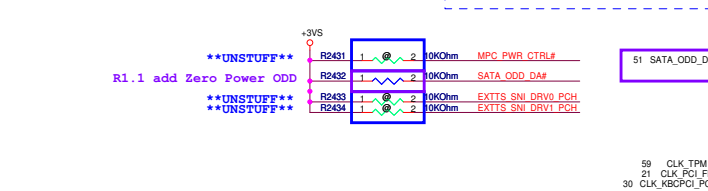
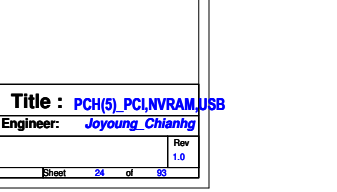
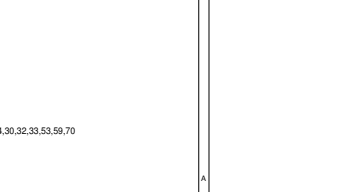
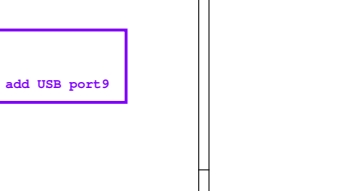
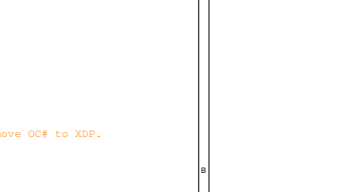
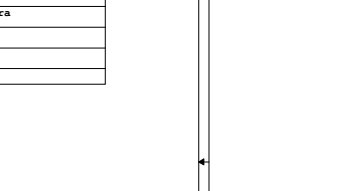
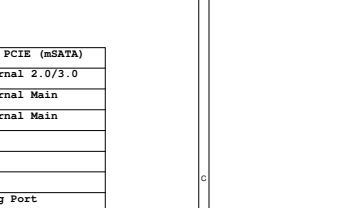
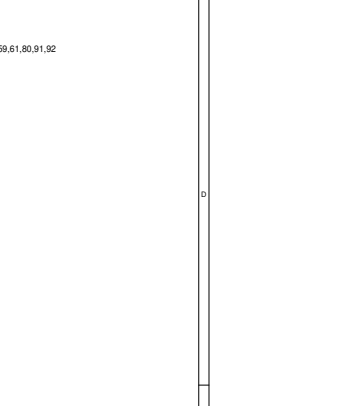
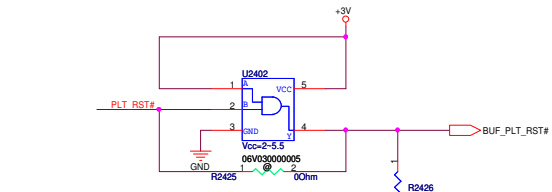
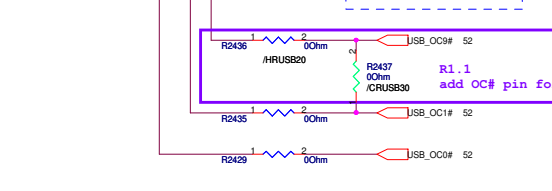
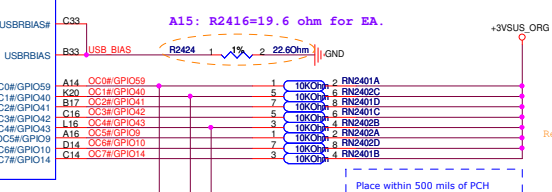
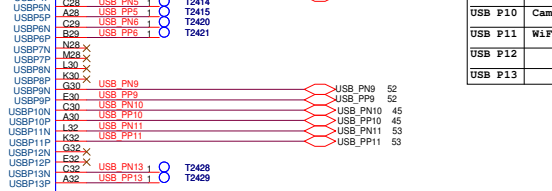
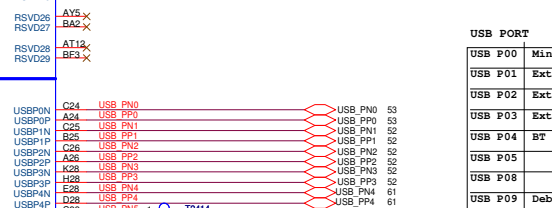
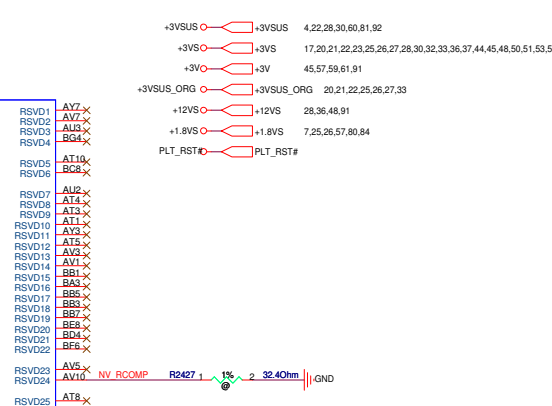
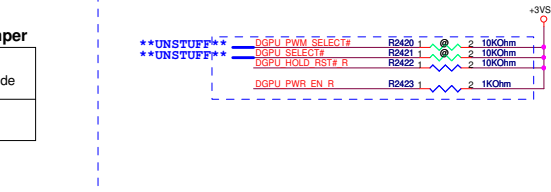
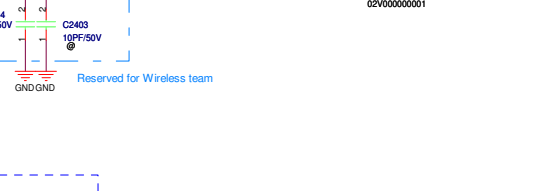
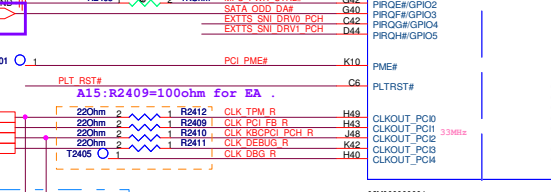
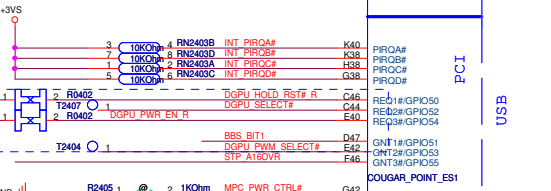
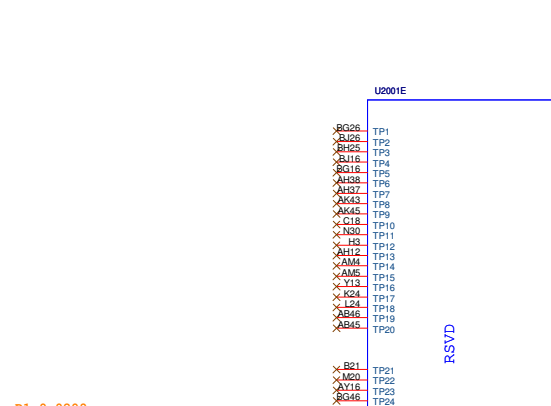
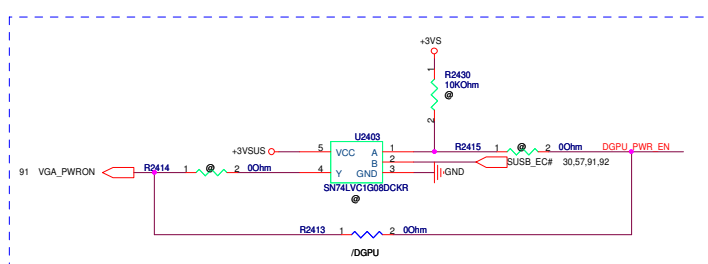


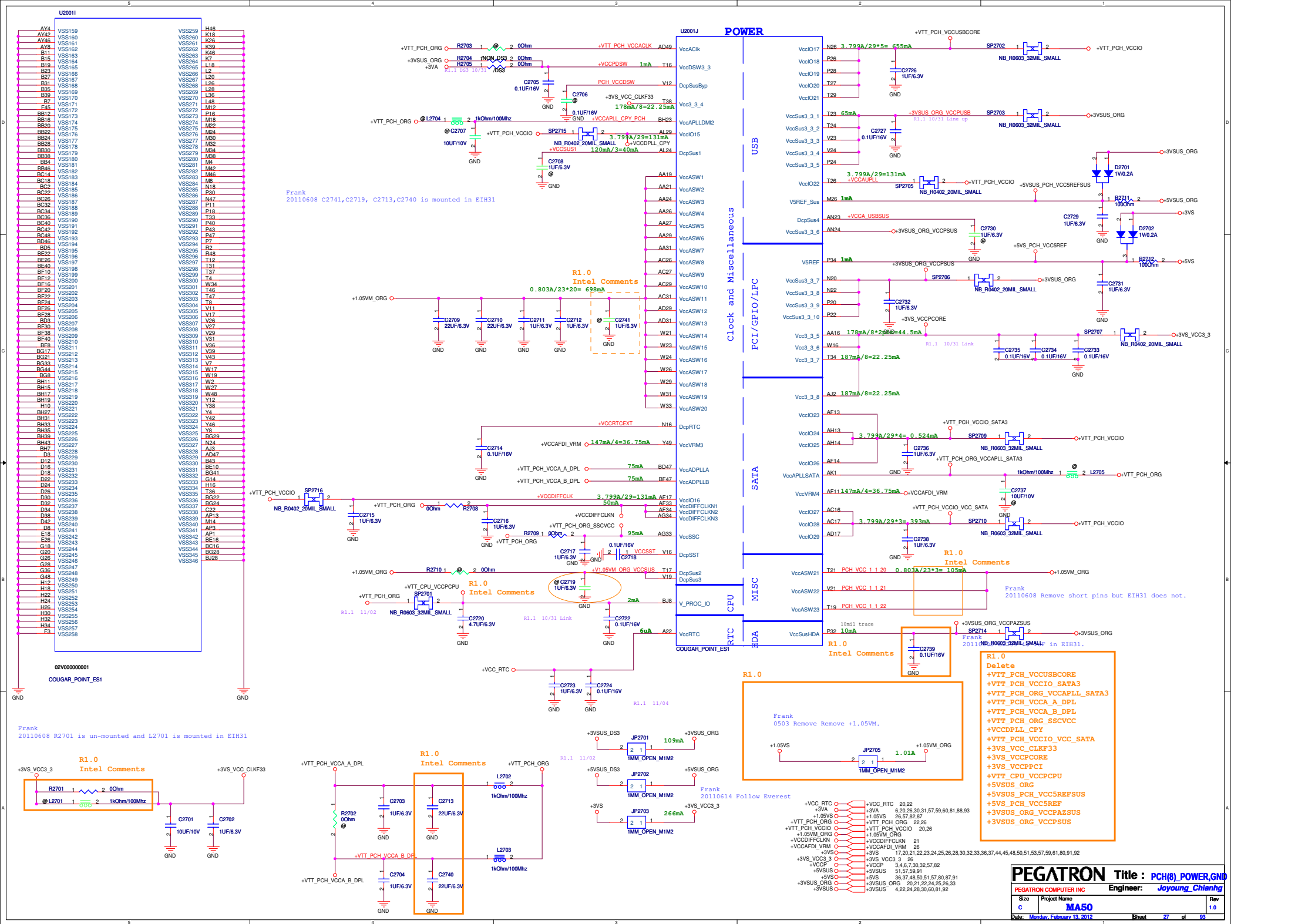
R1.0
Delete
+RTCBAT

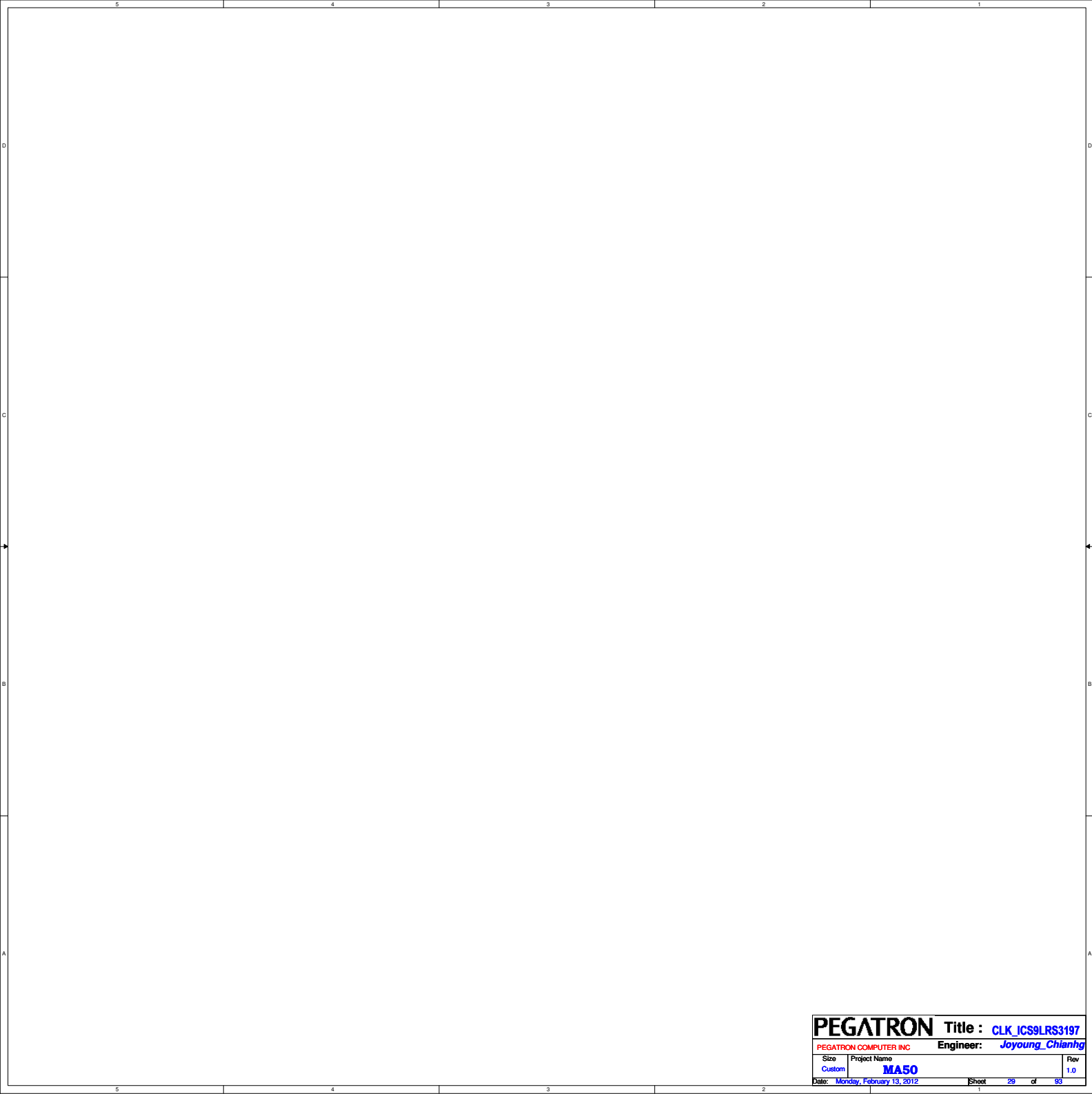


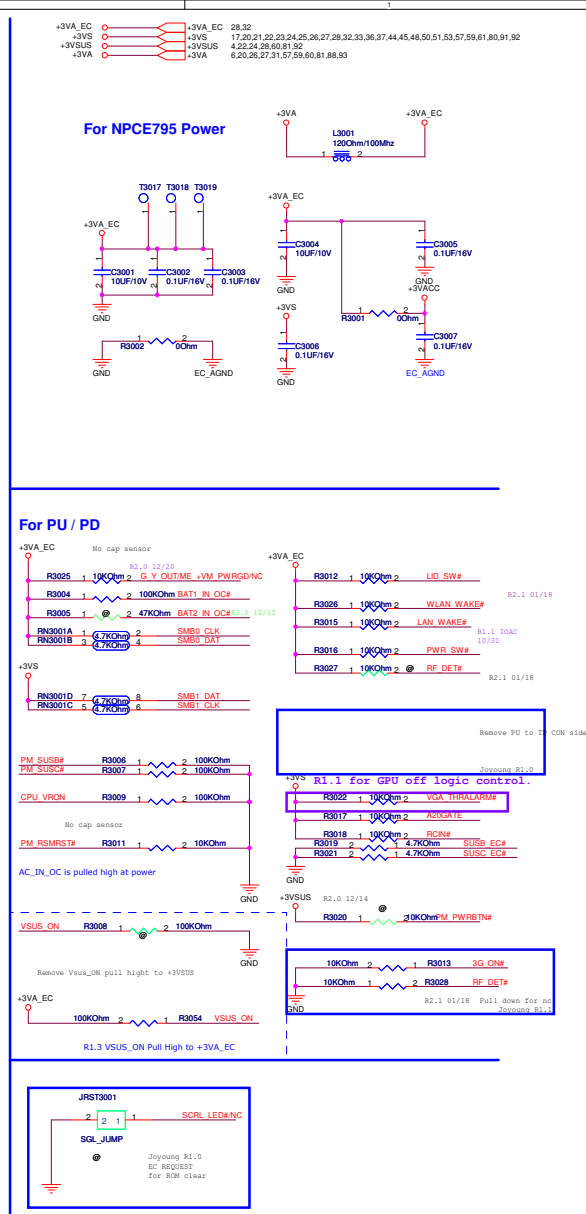
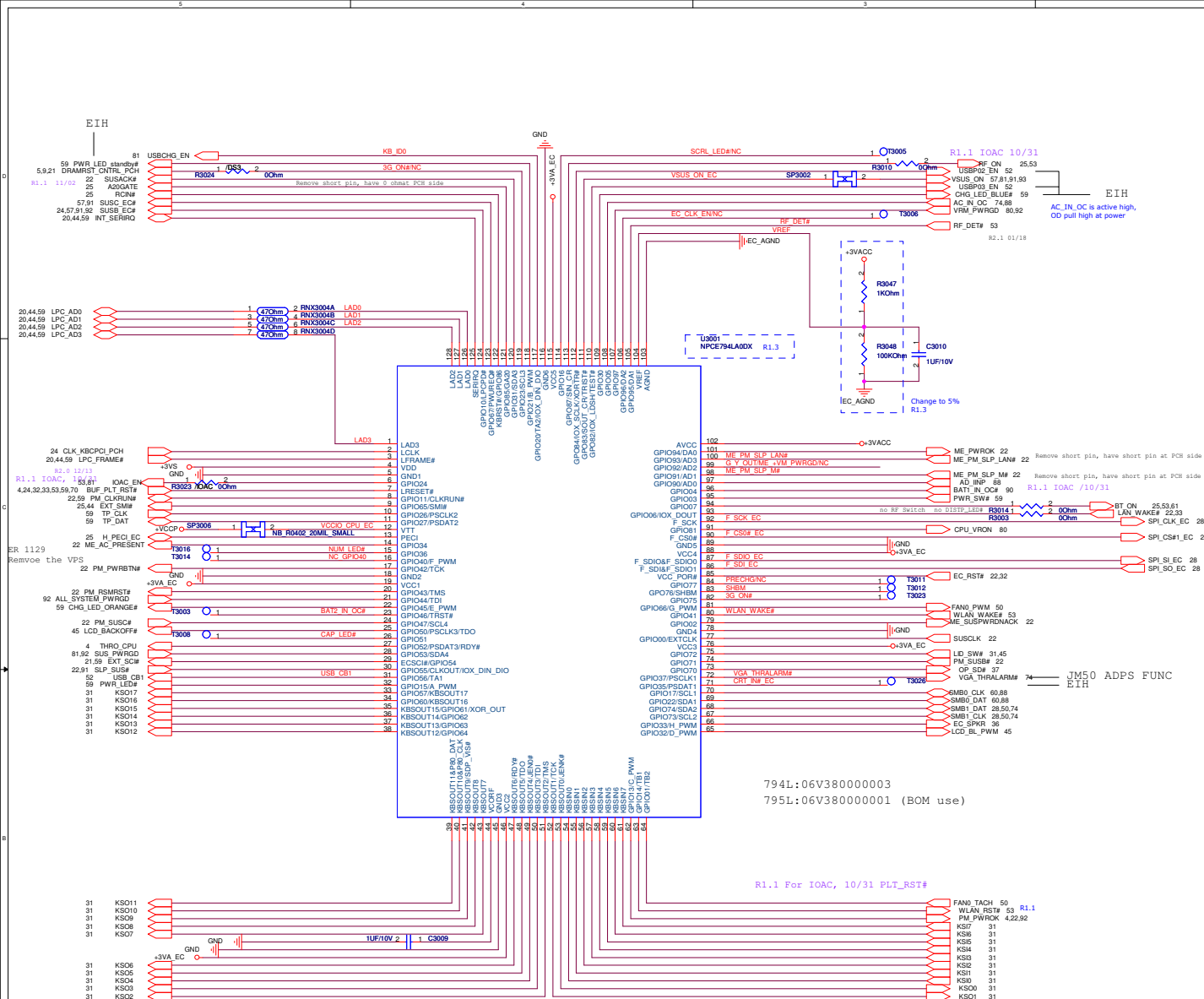
Frank
0517_Add 3G PCIE and CLKRQ in Port3.










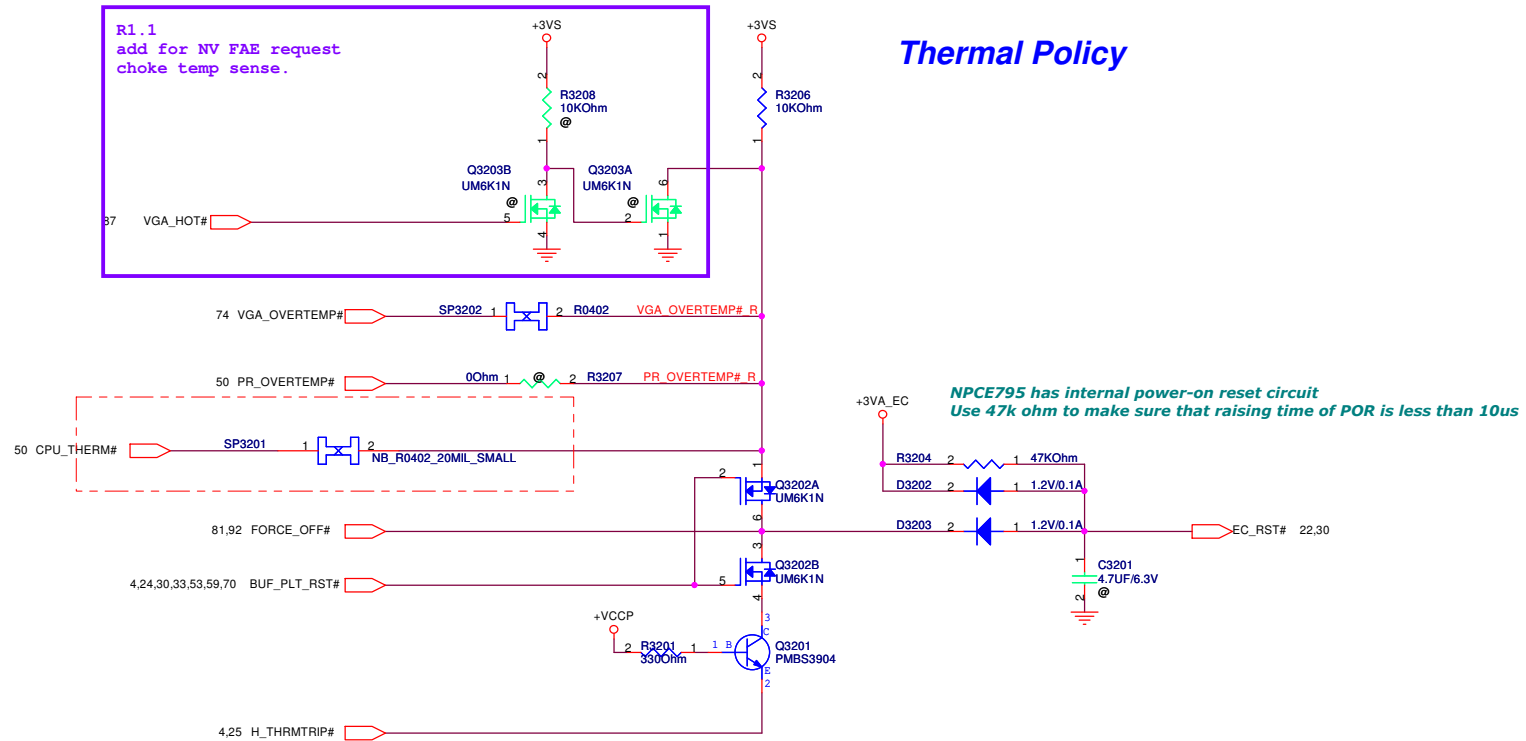


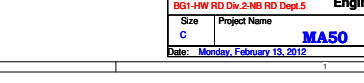
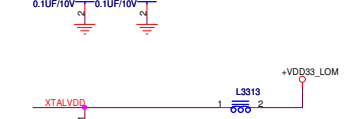
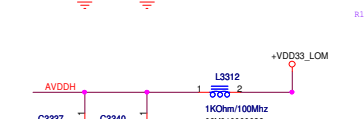
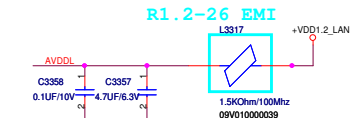
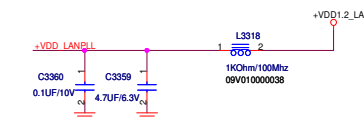
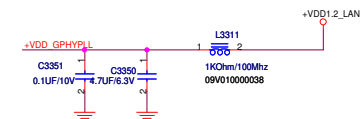
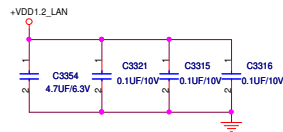
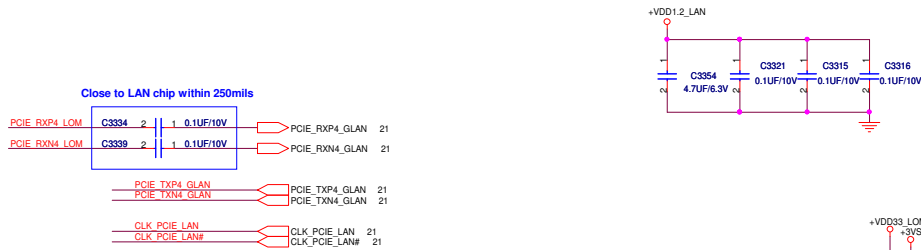




+VCCP  +VCCP 3,4,6,7,30,57,82
 +3VA_EC  +3VA_EC 28,30
 +3VS  +3VS 17,20,21,22,23,24,25,26,27,28,30,33,36,37,44,45,48,50,51,53,57,59,61,80,91,92

Thermal Policy





R1.0 Remove PU R for FAB suggestion.

R1.0 chnge VFRI.1.

Delete R5308 for unused.

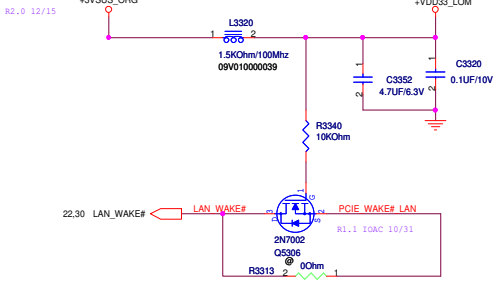
R1.1 change pin define.

R1.1 10/31 EMI CHANGE

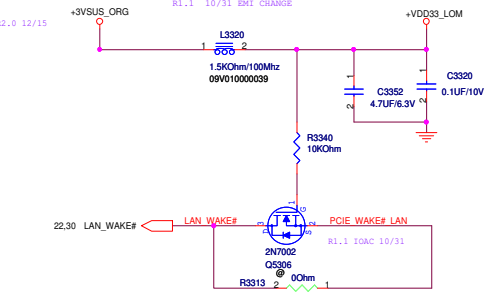
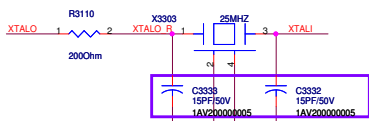
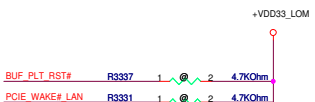
R1.0 OTP mode

R1.1 change value for -R test report

R1.1 10/31 EMI CHANGE



Frank 0503 LAN_LPWR is not defined GPIO in PCH.



Joyoung R1.0
FAE suggest common mode choke is on chip side.

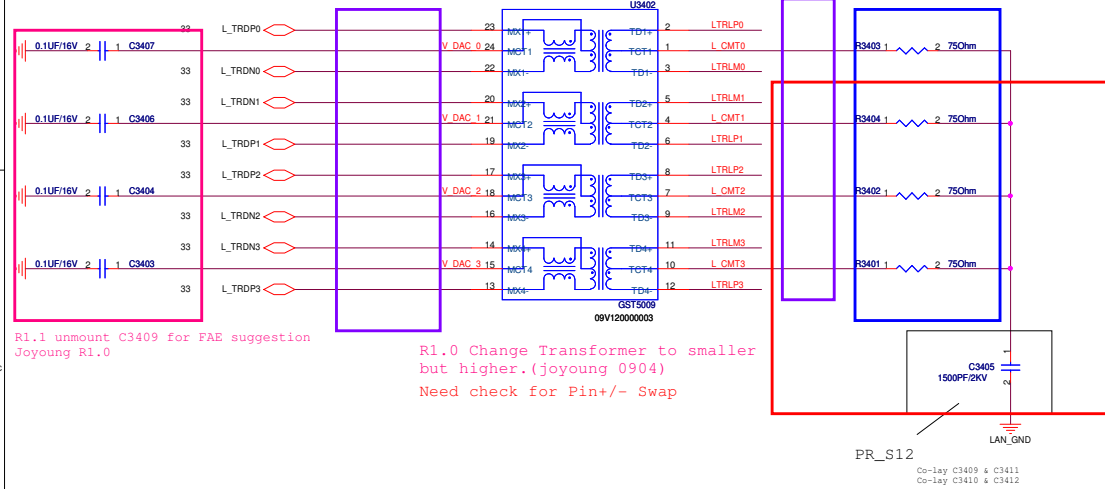
R1.1 Swap L_TRDP3 L_TRDN3 & L_TRDP1 L_TRDN1

R1.1 Add 0 OHM for FAE suggestion 0809
JM50: FAE suggest remove

R1.1 Mount R3401-R3403 for FAE suggestion 0809
R1.1 Remove R3405-R3407 & C3409

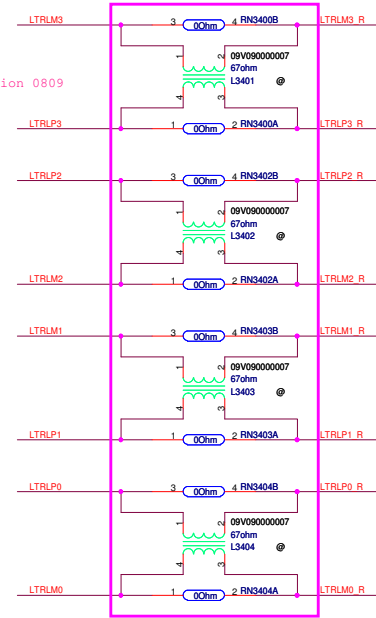
R1.1 remove CAP of V_DAC_3, V_DAC_2 and V_DAC_1 for FAE suggestion

R1.1 Remove R3405-R3407 & C3409

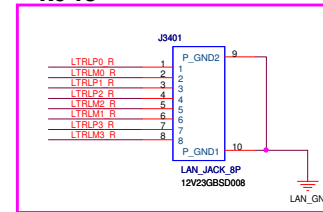


R1.1 unmount C3409 for FAE suggestion
Joyoung R1.0

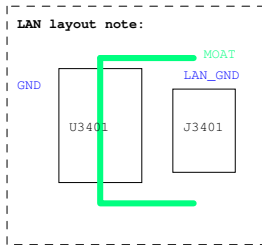
R1.0 Change Transformer to smaller
but higher.(joyoung 0904)
Need check for Pin+/- Swap



RJ45

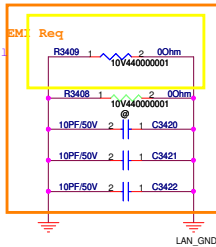


Change RJ45 CON3401

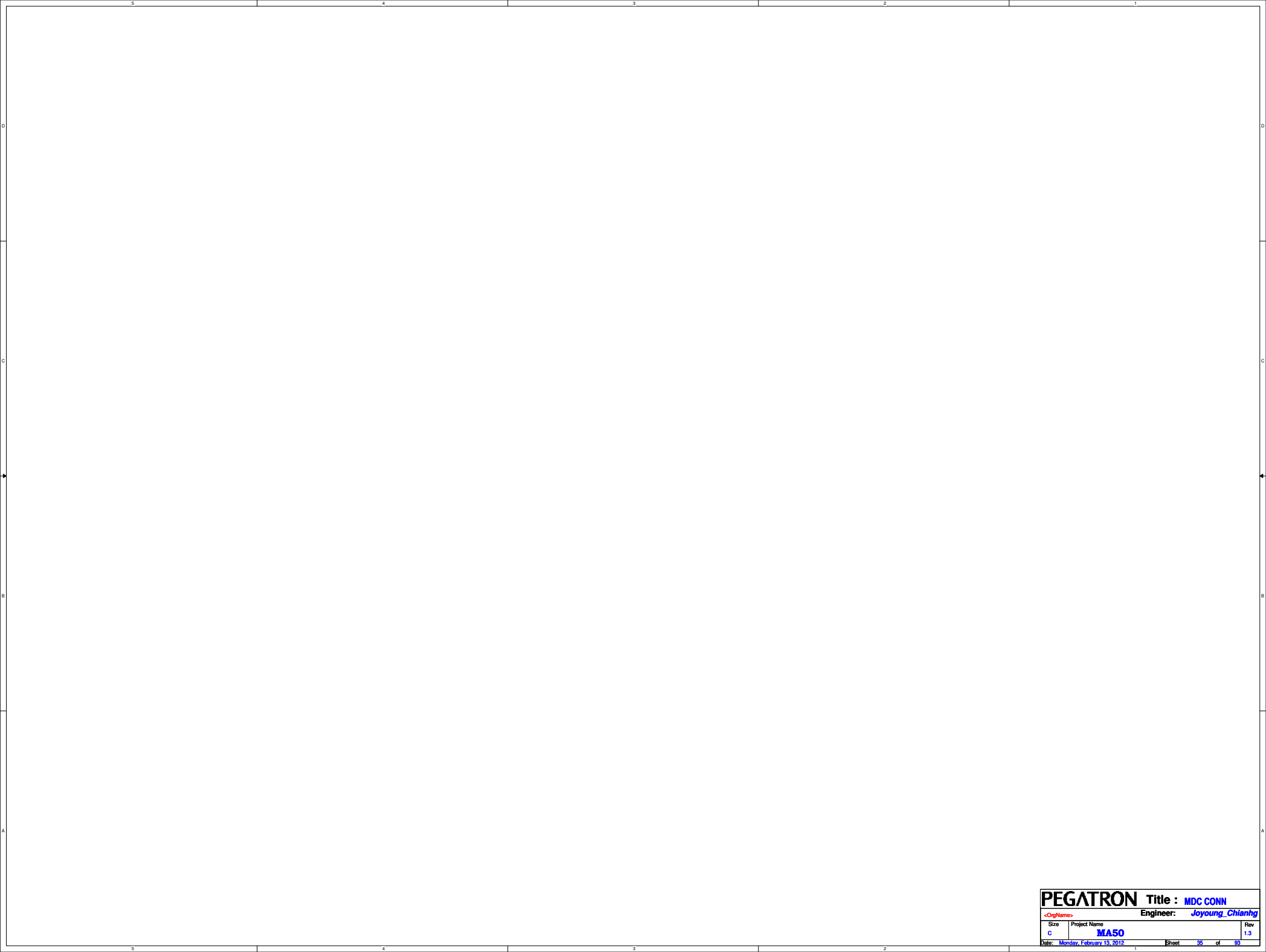


R1.0 Reserve D3401 for EMI.

R1.0 Mount R3408 for FAE suggestion



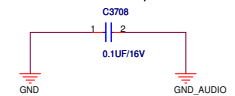
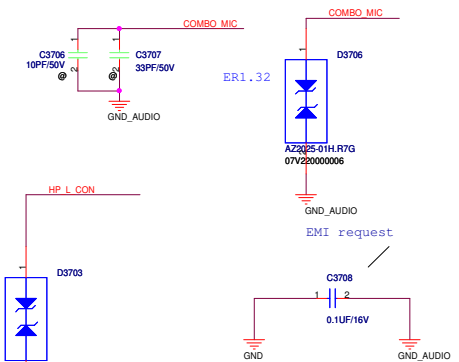
R1.1 EMI Request 4.7PF & Set Close to Connector, then removed all



PEGATRON		Title : MDC CONN	
<OrigName>		Engineer: Joyoung Chianhg	
Size	Project Name	Rev	
C	MA50	1.3	
Date: Monday, February 13, 2012		Sheet	35 of 83



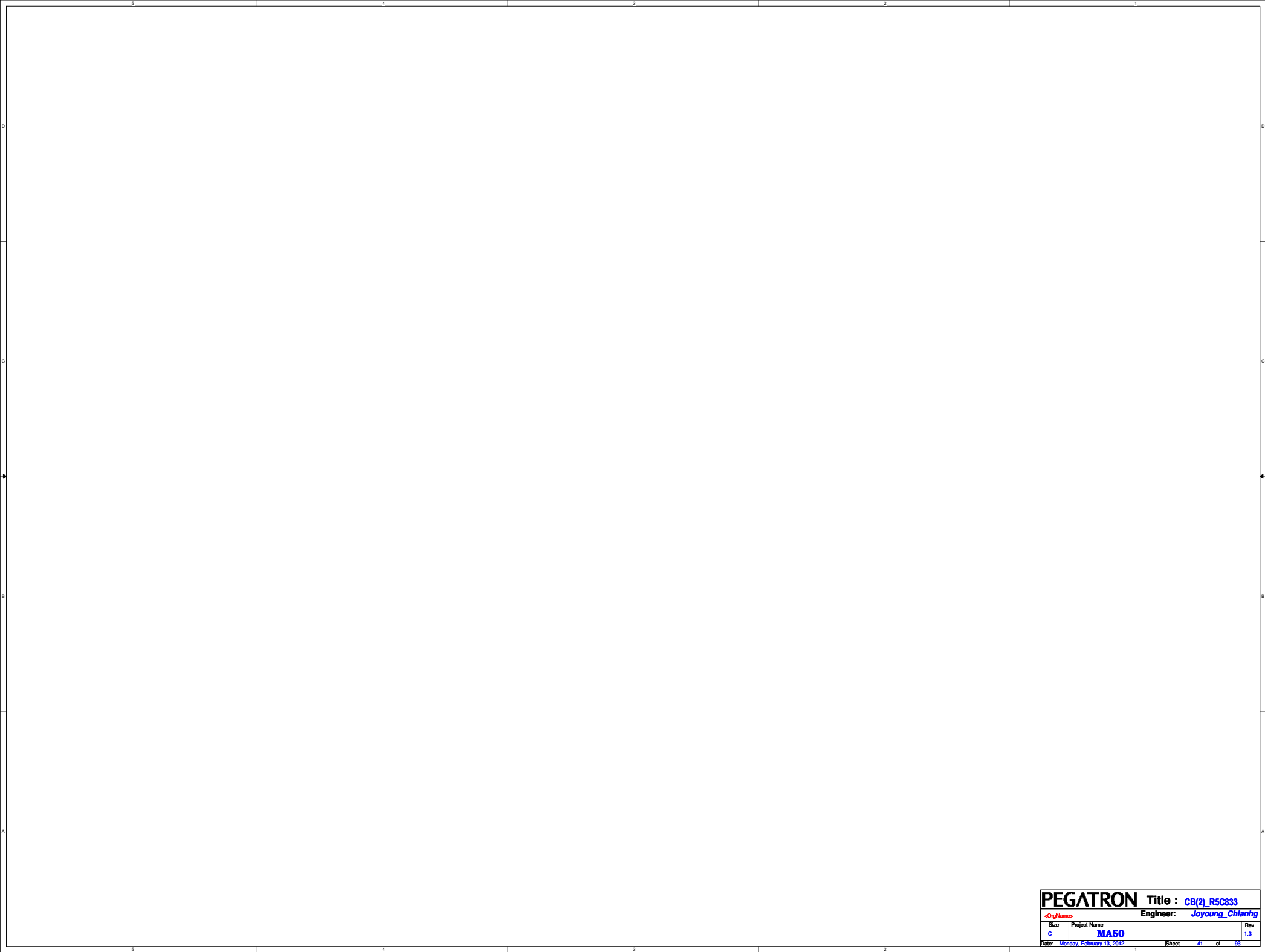
ER1.11







	5	4	3	2	1
D					
C					
B					
A					
	5	4	3	2	1

PEGATRON			Title : AUD(4)_****		
<OrgName>			Engineer: Joyoung_Chianhg		
Size	Project Name				Rev
Custom	MA50				1.3
Date:	Monday, February 13, 2012		Sheet	39	of 93

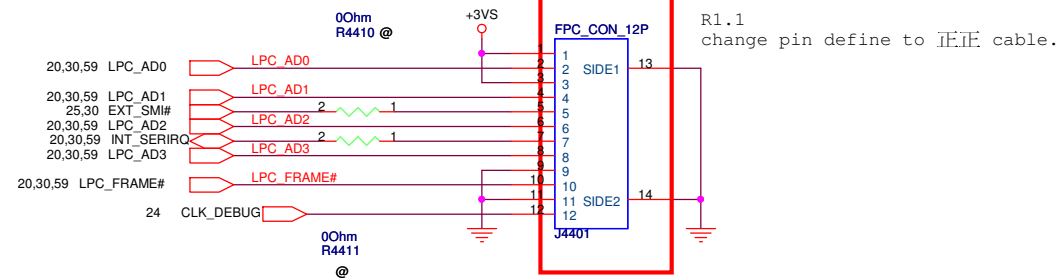


PEGATRON		Title : CB(2)_R5C833	
<OrgName>		Engineer: Joyoung_Chianhg	
Size	Project Name		Rev
C	MA50		1.3
Date: Monday, February 13, 2012		Sheet	41 of 83

+3VS  +3VS 17,20,21,22,23,24,25,26,27,28,30,32,33,36,37,44,45,48,50,51,53,57,59,61,80,91,92
+12V  +12V 60,91

+3VS  +3VS 17,20,21,22,23,24,25,26,27,28,30,32,33,36,37,45,48,50,51,53,57,59,61,80,91,92

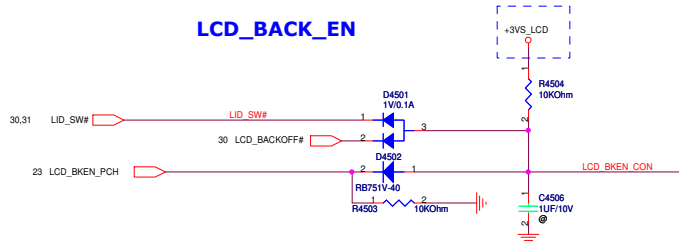
LPC Debug Port



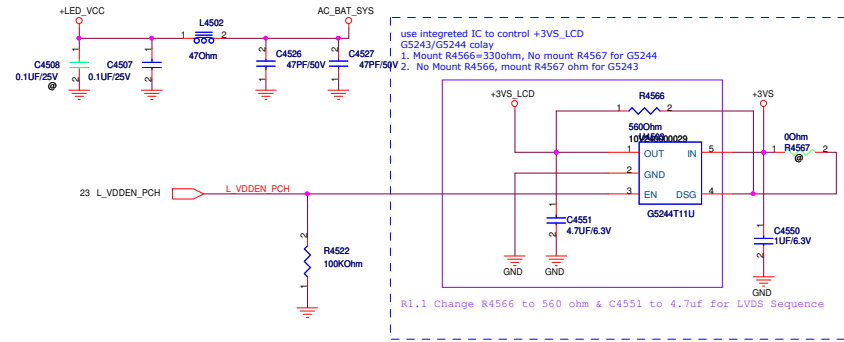
PEGATRON		Title : BUG_Debug	
<OrgName>		Engineer: Joyoung_Chianhg	
Size	Project Name		Rev
B	MA50		1.3
Date: Monday, February 13, 2012		Sheet 44	of 93

+3VS	17,20,21,22,23,24,25,26,27,28,30,32,33,36,37,44,48,50,51,53,57,59,61,80,91,92
+5VS	27,36,37,48,50,51,57,80,87,91
+12VS	28,36,48,91
+VCCP	3,4,6,7,30,32,57,82
AC_BAT_SYS	53,81,87,88

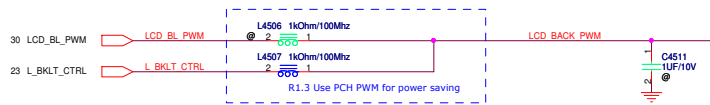
LCD_BACK_EN



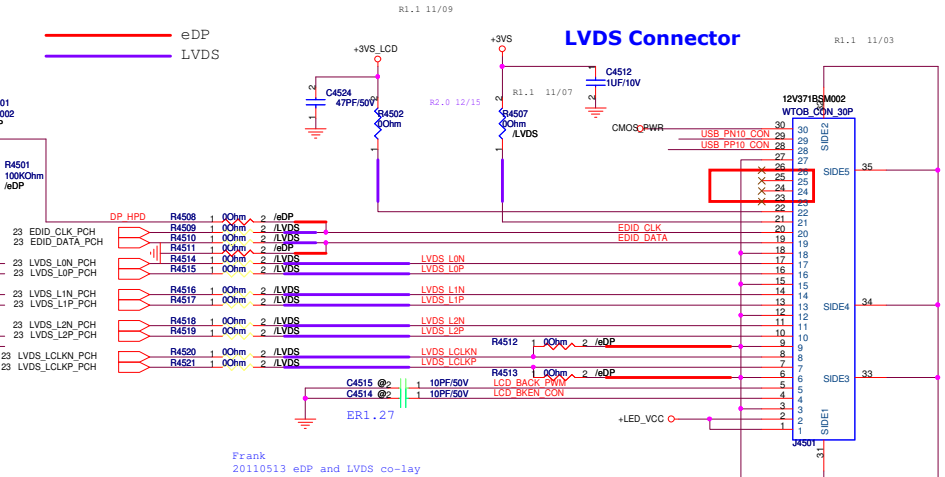
LCD VDDEN / +LED_VCC



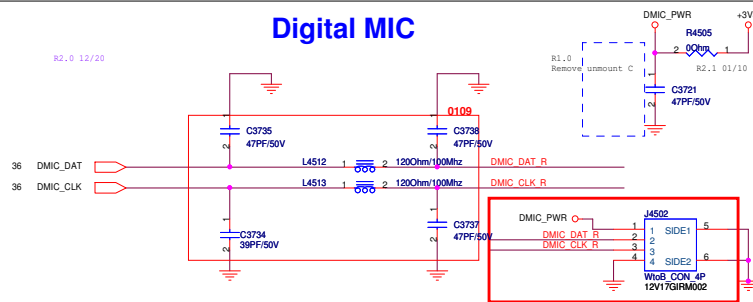
LCD_BL_PWM



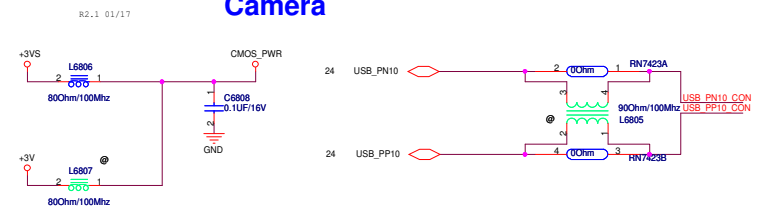
eDP
LVDS



Digital MIC

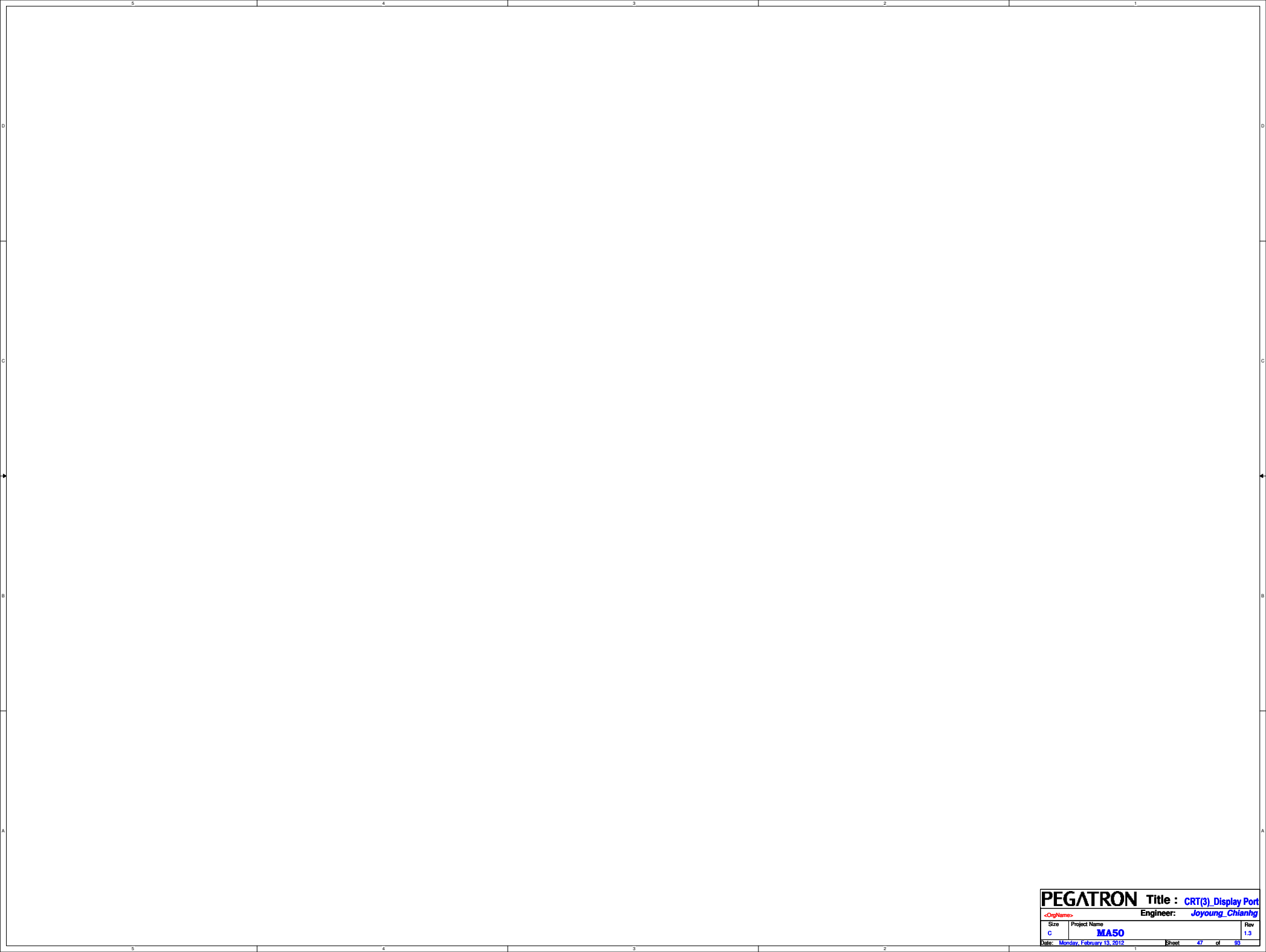


Camera

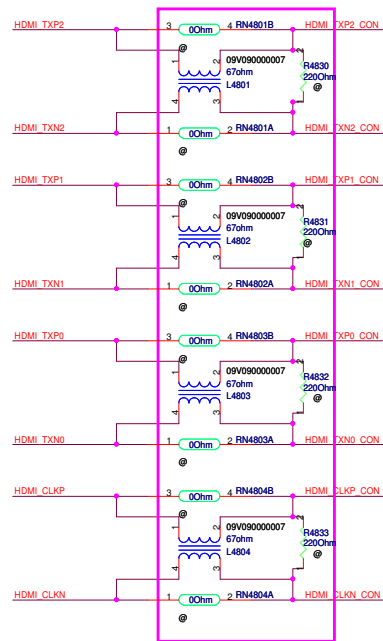
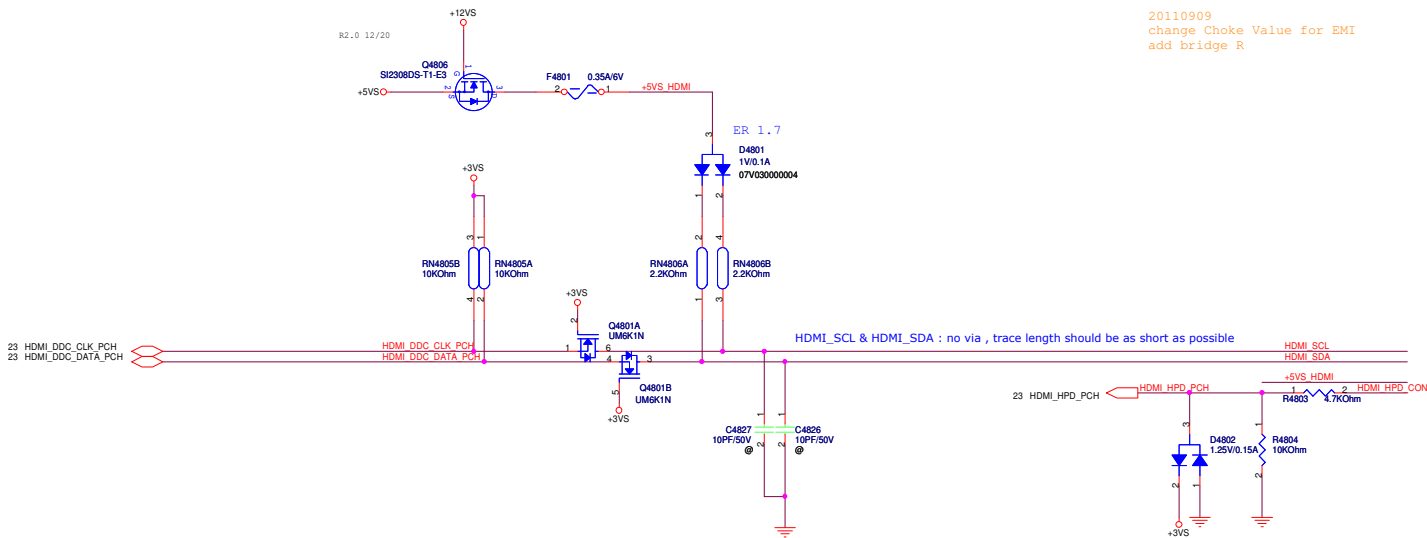
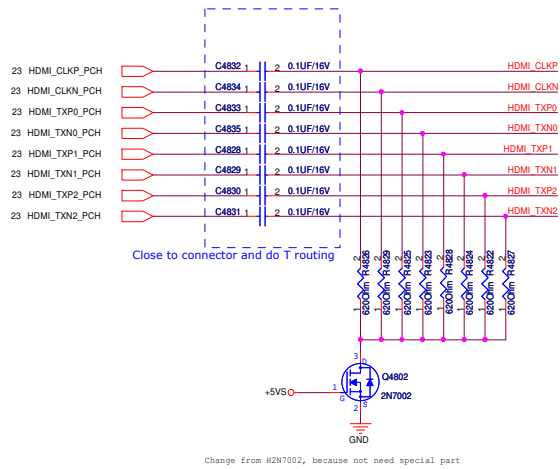




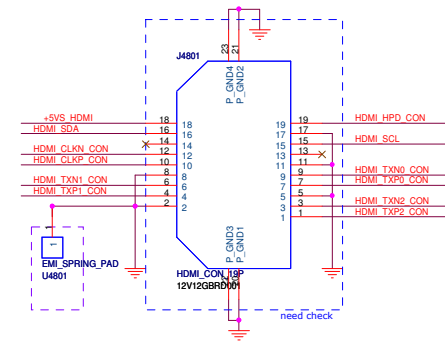
PEGATRON		Title : CRT	
BU1-RD Div.1-HW RD Dept.1		Engineer: <i>Joyoung_Chianhg</i>	
Size Custom	Project Name MA50		Rev 1.0
Date: <i>Monday, February 13, 2012</i>		Sheet	46 of 93



PEGATRON		Title : CRT(3)_Display Port	
<OrgName>		Engineer: Joyoung_Chianhg	
Size	Project Name		Rev
C	MA50		1.3
Date: Monday, February 13, 2012		Sheet	47 of 83



20110909
change Choke Value for EMI
add bridge R



R1.1 EMI Request for Spring PAD(close to HDMI conn)

+12VS	+12VS	28,36,91
+3VS	+3VS	17,20,21,22,23,24,25,26,27,28,30,32,33,36,37,44,45,50,51,53,57,59,61,80,91,92
+5VS	+5VS	27,36,37,50,51,57,80,87,91

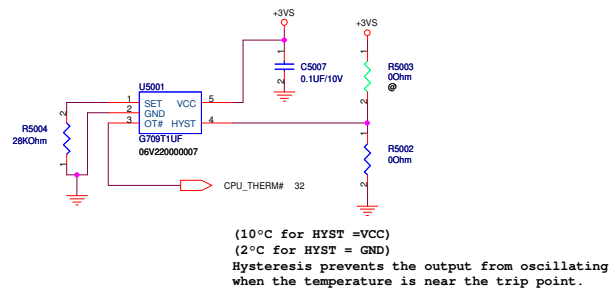
PEGATRON		Title : TV(1)_HDMI	
<OrigName>		Engineer: Joyoung Chianhg	
Size	Project Name	Rev	
C	MA50	1.3	
Date: Monday, February 13, 2012	Sheet	46	of 93



PEGATRON		Title : TV(2)_****	
<OrigName>		Engineer: Joyoung_Chianhg	
Size	Project Name		Rev
C	MA50		1.3
Date: Monday, February 13, 2012		Sheet	49 of 83

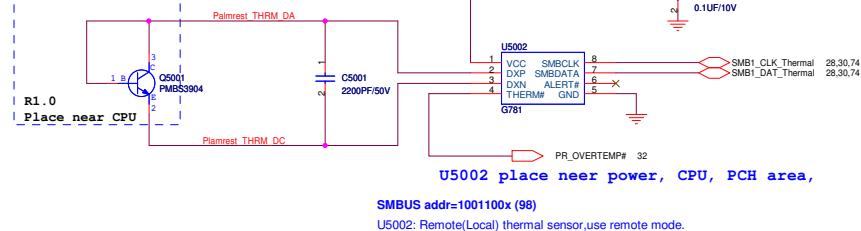
+3VS 17,20,21,22,23,24,25,26,27,28,30,32,33,36,37,44,45,48,51,53,57,59,61,80,91,92
+5VS 27,36,37,48,51,57,80,87,91

CPU Thermal Sensor

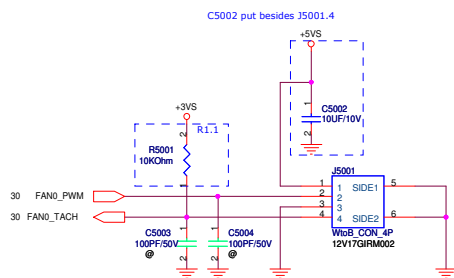


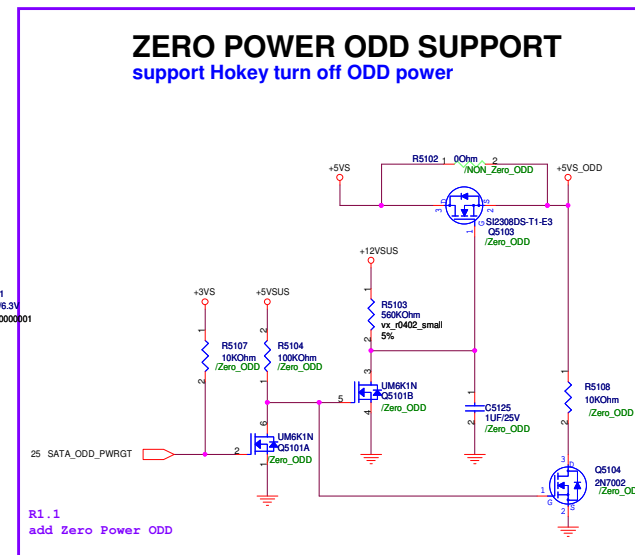
DIMM Thermal Sensor

PHILIP PMBS3904
Please in the center of Plamrest.



PWM Fan



[illegible]

PEGATRON		Title : <u>XDD_HDD,ODD</u>	
<OrigName>		Engineer: <u>Joyoung_Chianhg</u>	
Size C	Project Name MA50	Rev 1.3	
Date: <u>Monday, February 13, 2012</u>		Sheet	51 of 93

PEGATRON		Title : <u>USB3.0</u>	
<OrgName>		Engineer: <u>Joyoung_Chianhg</u>	
Size B	Project Name MA50	Rev 1.3	
Date: <u>Monday, February 13, 2012</u>		Sheet	54 of 93





+3VA 6,20,26,27,30,31,57,59,60,81,88,93
+3VS 17,20,21,22,23,24,25,26,27,28,30,32,33,36,37,44,45,48,50,51,53,57,59,61,80,91,92
+5VSUS 51,57,59,91
+5VA 37,60,81,91
+5V 57,59,60,91
+5VS 27,36,37,48,50,51,57,80,87,91
AC_BAT_SYS AC_BAT_SYS 45,53,81,87,88
+3V 24,45,57,59,61,91

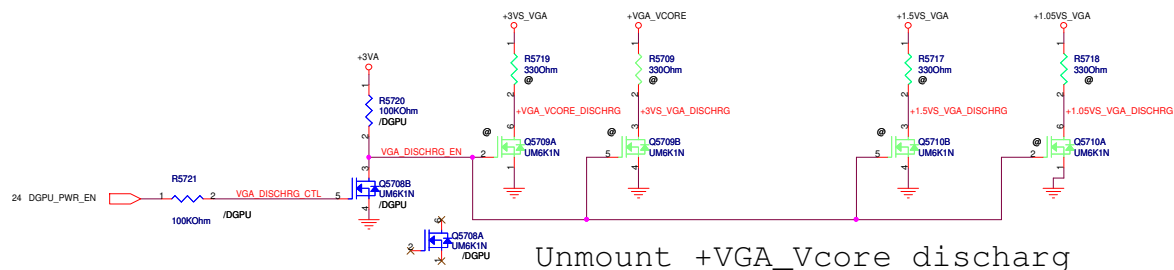
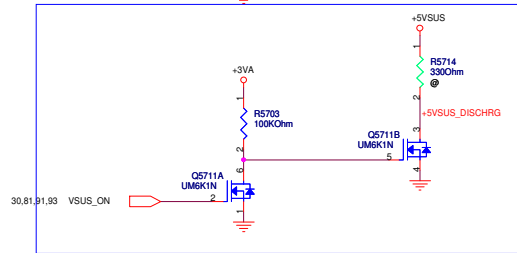
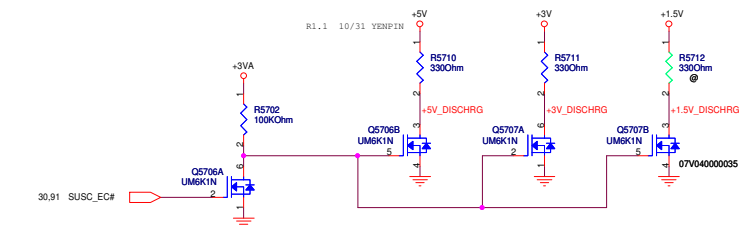
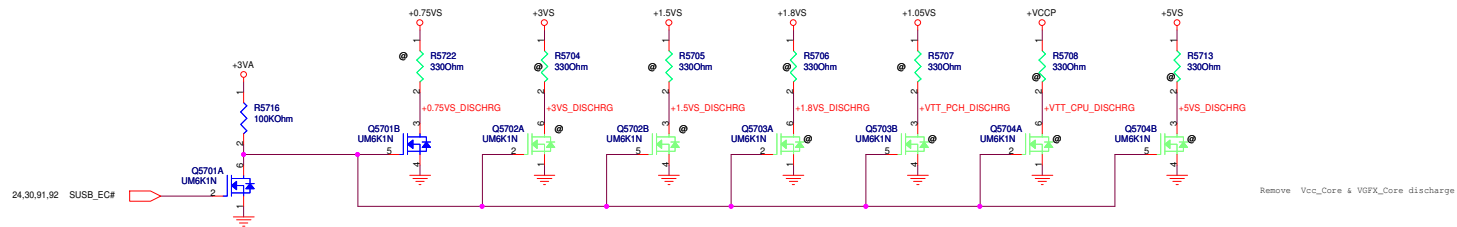
30.59 PWR_LED#

30.59 PWR_LED_standby#

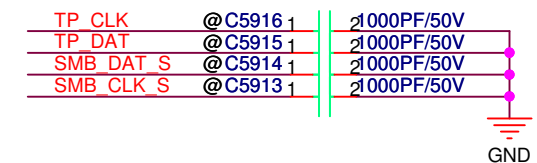
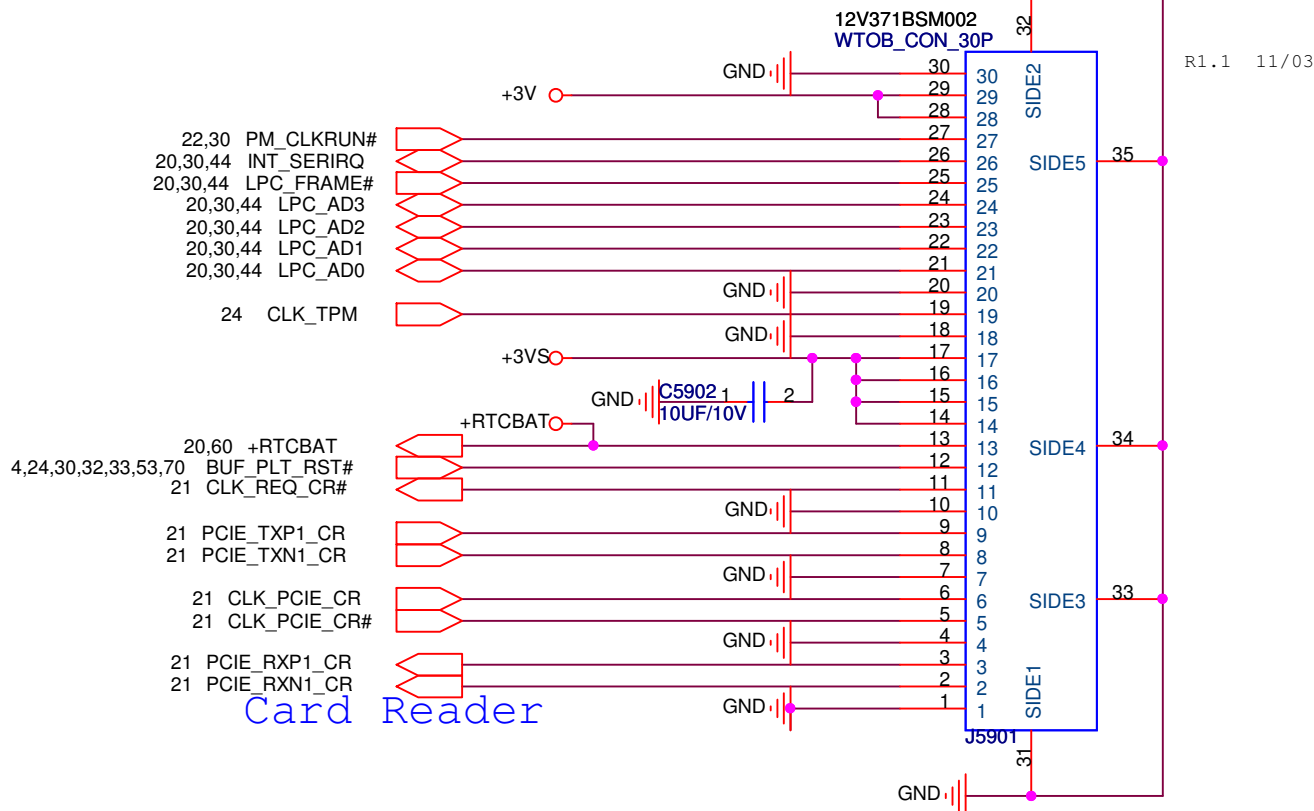
30.59 CHG_LED_BLUE#

30.59 CHG_LED_ORANGE#

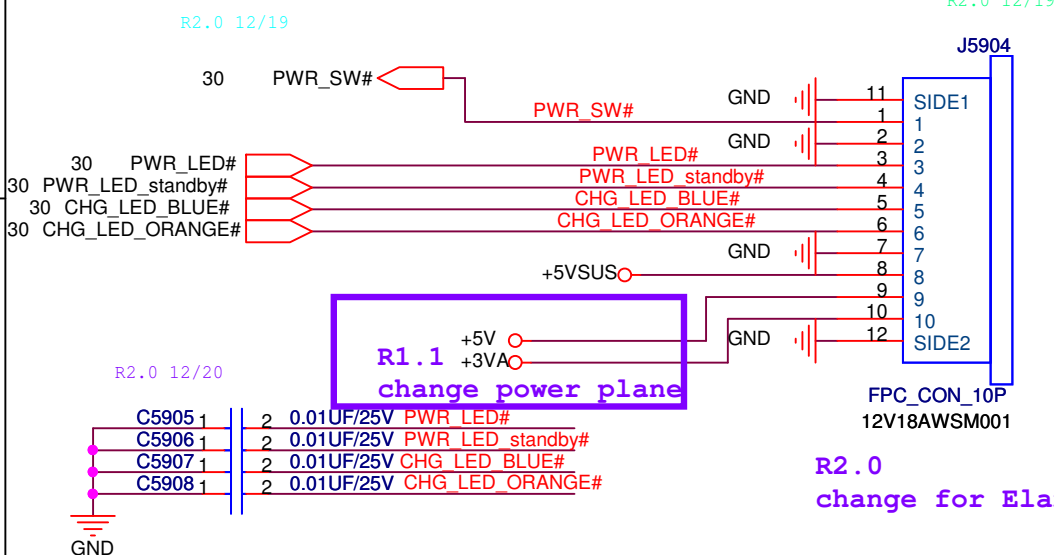
+3VA	6,20,26,27,30,31,59,60,81,88,93
+VOCORE	6,9,11,80
+VGFX_CORE	7,9,80
+VCCP	3,4,6,7,30,32,82
+0.75VS	16,17,83
+1.05VS	26,27,82,87
+1.5VS	7,26,53,91
+1.8VS	7,25,26,80,84
+3VS	17,20,21,22,23,24,25,26,27,28,30,32,33,36,37,44,45,48,50,51,53,59,61,80,91,92
+5VS	27,36,37,48,50,51,80,87,91
+1.5V	5,16,17,18,60,83
+3V	24,45,59,61,91
+5V	59,60,91



PEGATRON		Title : System Setting	
<OrgName>		Engineer: <i>Joyoung_Chianhg</i>	
Size	Project Name		Rev
Custom	MASO		1.3
Date: <i>Monday, February 13, 2012</i>		Sheet	58 of 93

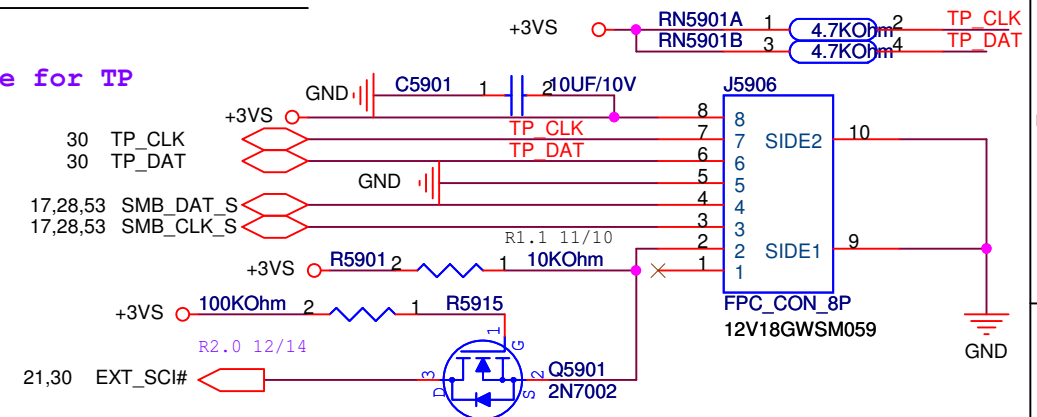


Power BTN and LED



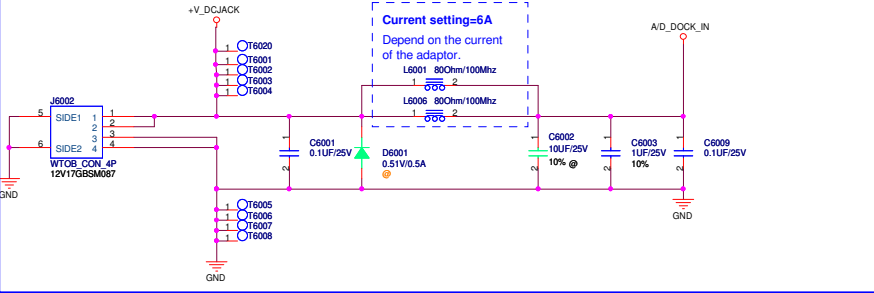
R1.1

change for TP

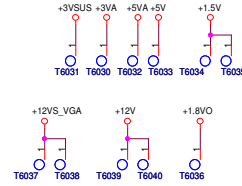
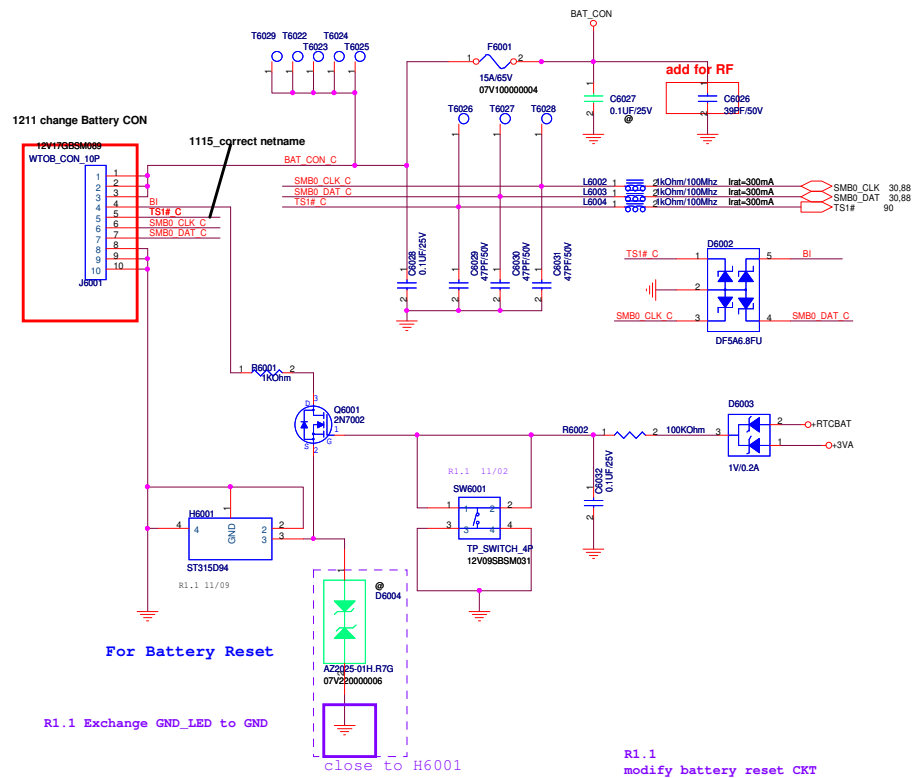


PEGATRON			Title : B to B		
<OrgName>			Engineer: Joyoung_Chianhg		
Size A	Project Name MA50			Rev 1.3	
Date: Monday, February 13, 2012		Sheet 59		of 93	

DC Jack WtoB CONN



Battery Connector

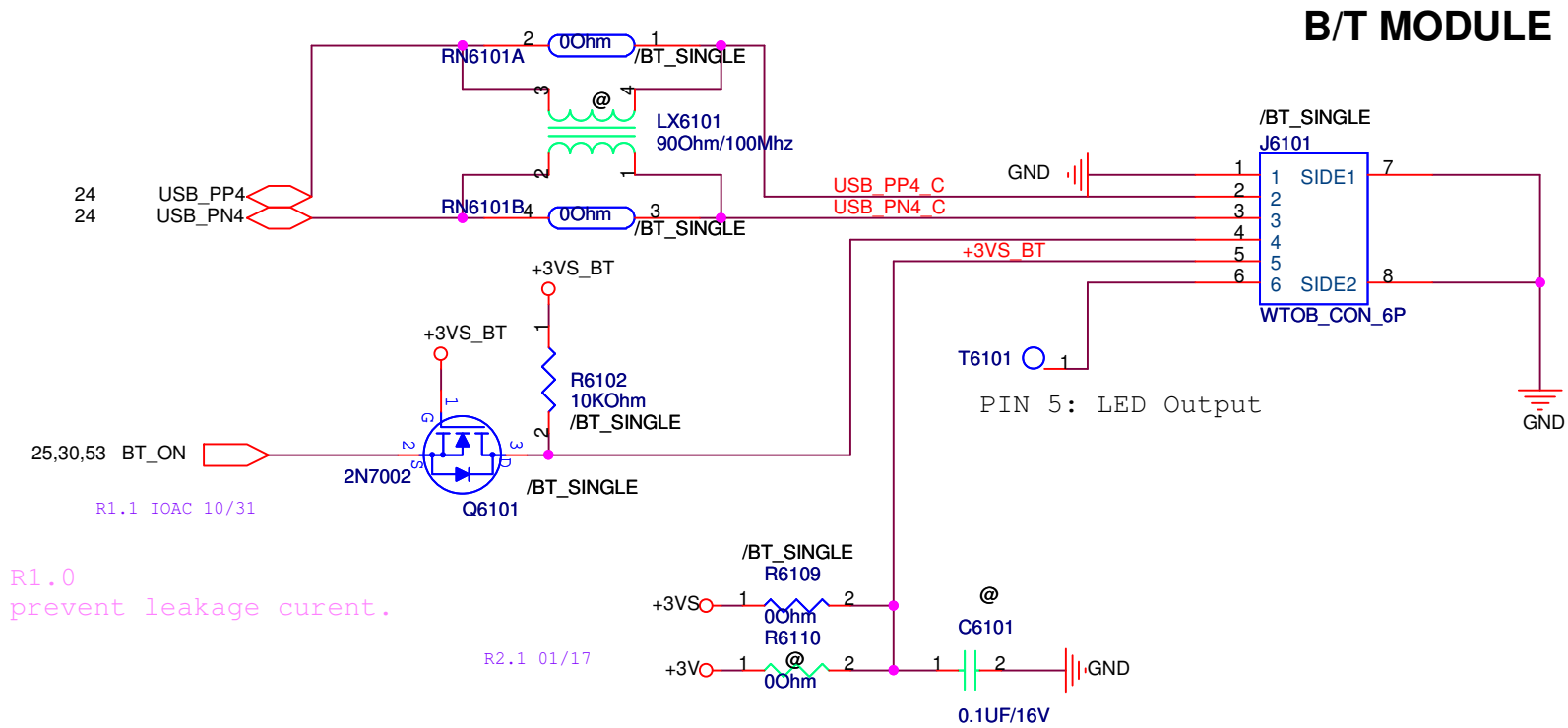


+VCC_RTC	+VCC_RTC	20,22,27
+3VA_EC	+3VA_EC	28,30,32
+3VA	+3VA	6,20,26,27,30,31,57,59,81,88,93
+5VA	+5VA	37,81,91
+3VSUS	+3VSUS	4,22,24,28,30,81,92
+5VSUS	+5VSUS	51,57,59,91
+12VSUS	+12VSUS	28,51,81,91
+1.5V	+1.5V	5,16,17,18,57,83
+3V	+3V	24,45,57,59,61,91
+5V	+5V	57,59,91
+12V	+12V	91
+0.75VS	+0.75VS	16,17,57,83
+1.05VS	+1.05VS	26,27,57,82,87
+1.5VS	+1.5VS	7,26,53,57,91
+1.8VS	+1.8VS	7,25,26,57,80,84
+3VS	+3VS	17,20,21,22,23,24,25,26,27,28,30,32,33,36,37,44,45,48,50,51,53,57,59,61,80,91,92
+5VS	+5VS	27,36,37,48,50,51,57,80,87,91
+12VS	+12VS	28,36,48,91

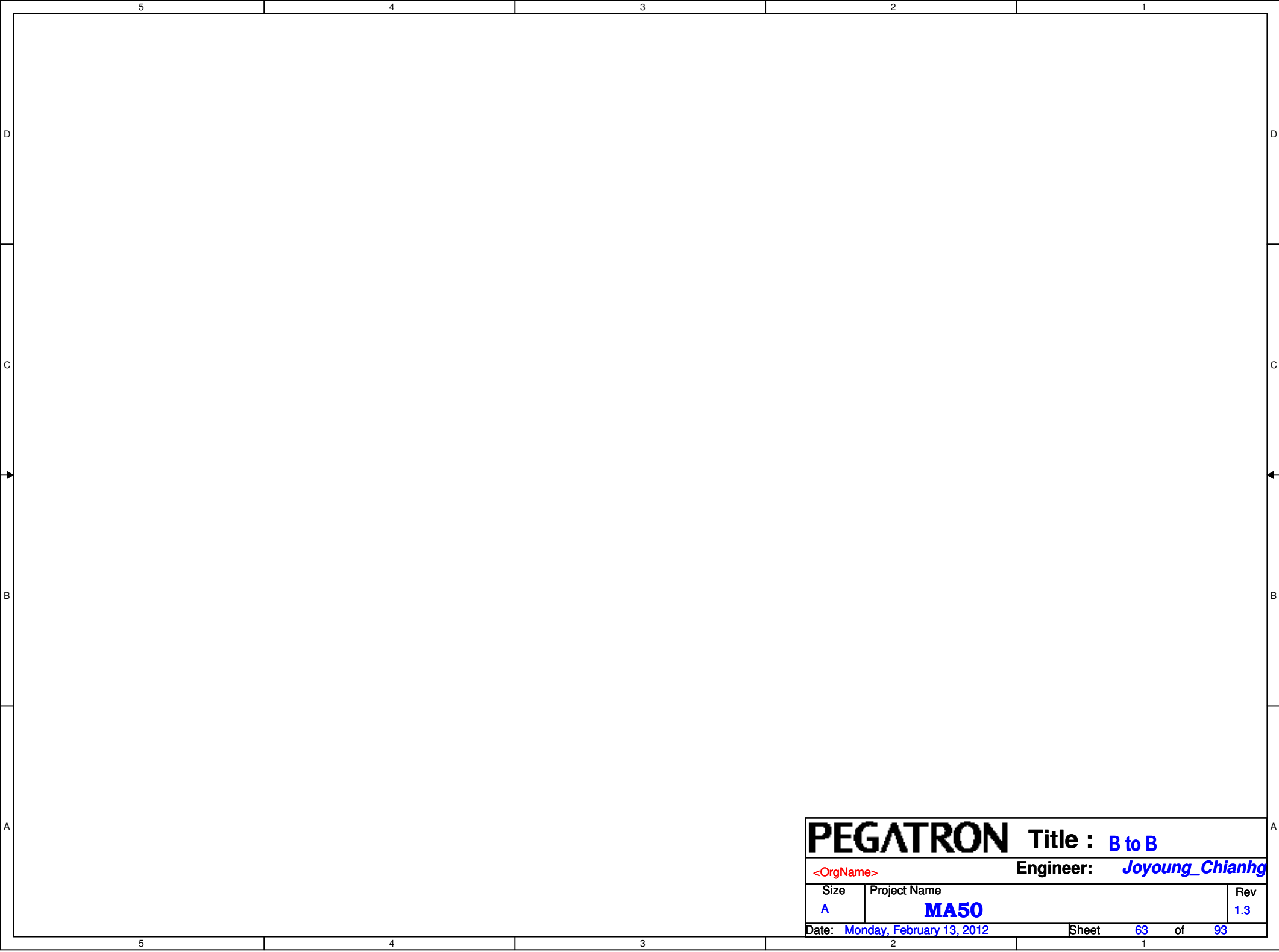
AC_BAT_SYS	AC_BAT_SYS	45,53,81,87,88
A/D_DOCK_IN	A/D_DOCK_IN	88
BAT_CON	BAT_CON	88

+VCCP	+VCCP	3,4,6,7,30,32,57,82
+VCORE	+VCORE	6,9,11,80
+VGFX_CORE	+VGFX_CORE	7,9,80
+VTT_PCH_ORG	+VTT_PCH_ORG	22,26,27
+VTT_PCH_VCCIO	+VTT_PCH_VCCIO	20,26,27
+1.05VM_ORG	+1.05VM_ORG	27

+V_VREF_DDR3	+V_VREF_DDR3	16,17,18
--------------	--------------	----------

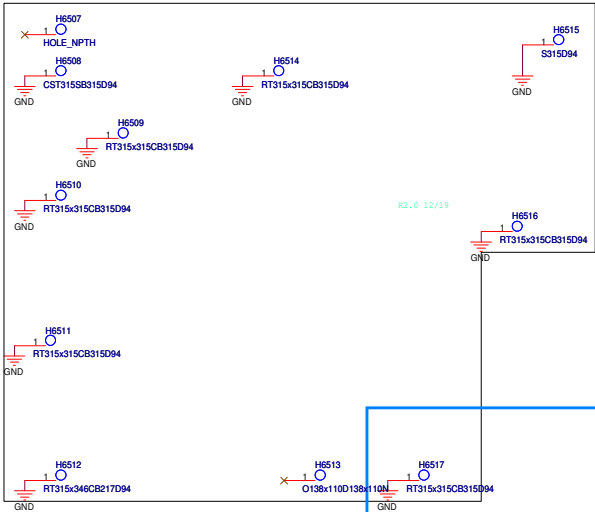
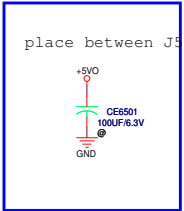
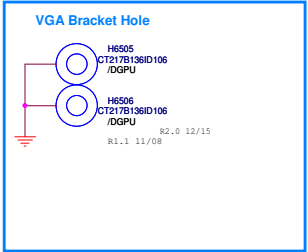
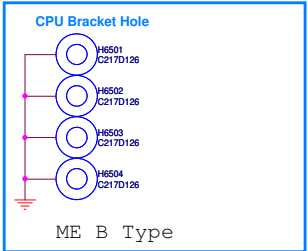


PEGATRON		Title : System Setting	
<OrgName>		Engineer: <i>Joyoung_Chianhg</i>	
Size	Project Name		Rev
Custom	MASO		1.3
Date: <i>Monday, February 13, 2012</i>		Sheet	62 of 93

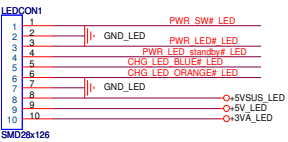


PEGATRON			Title : B to B		
<OrgName>			Engineer: Joyoung_Chianhg		
Size	Project Name				Rev
A	MA50				1.3
Date: Monday, February 13, 2012			Sheet	63	of 93

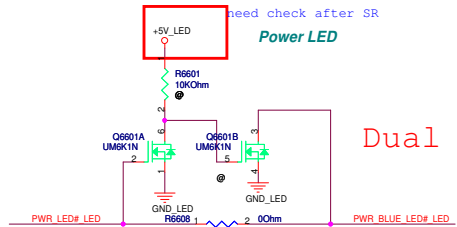
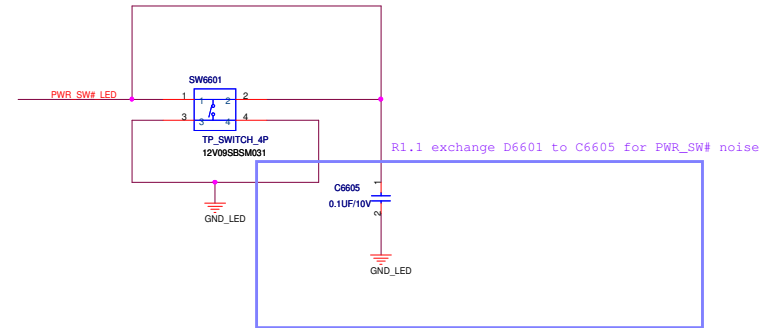




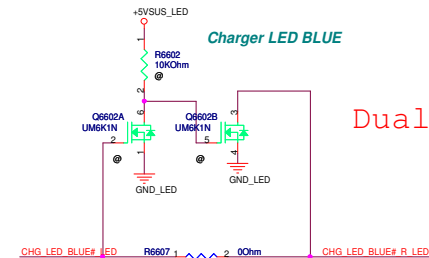
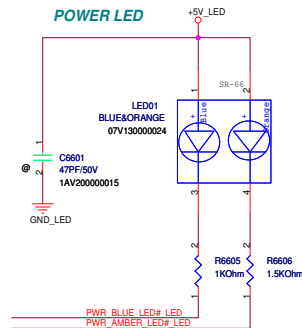
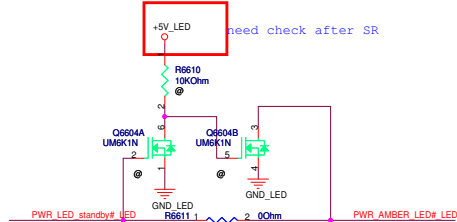
This screw hole should be Upside down(TOP and BOTTOM) .



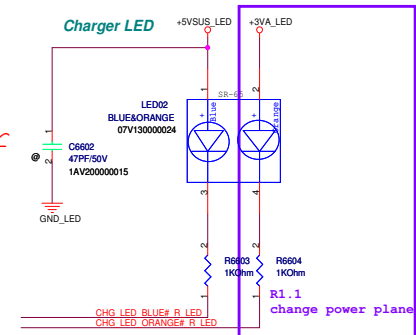
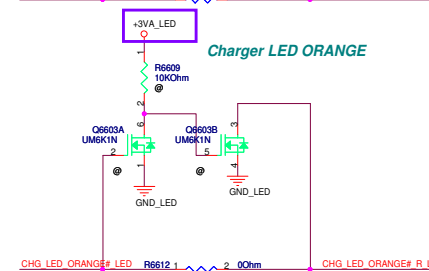
Power Button

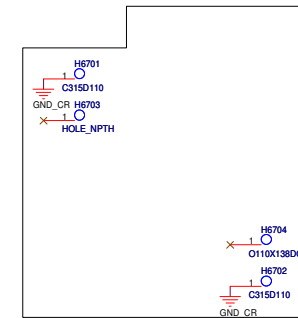


Dual Color



Dual Color

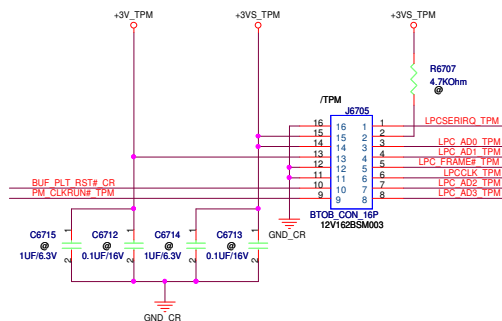
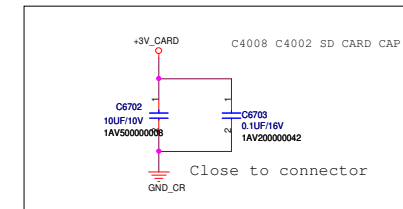
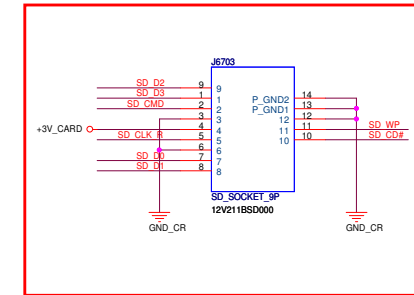
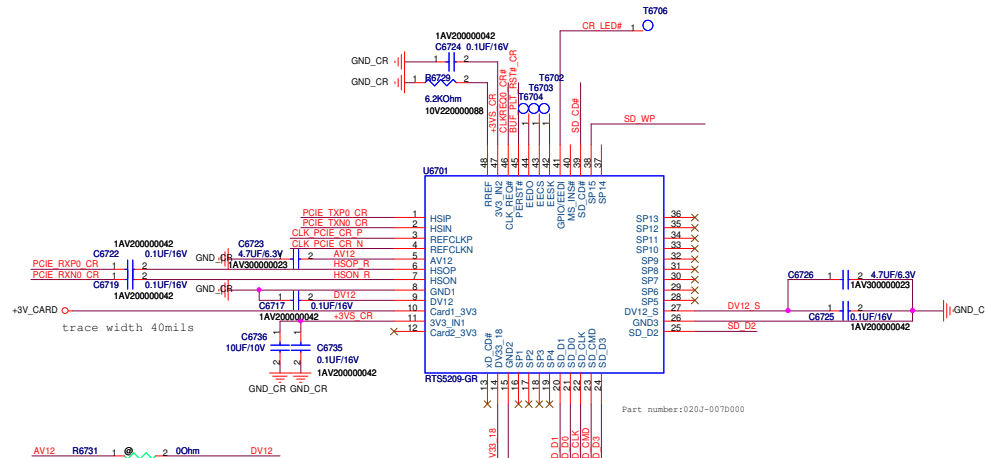
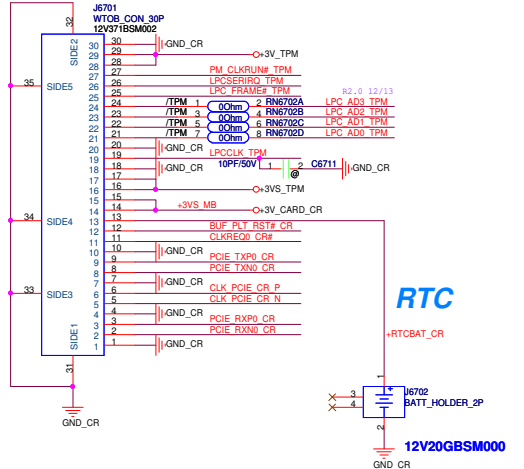




SDCLK trace length
shorter, surround with GND.

From System's PCIE interface

R1.1 change to 30P



Remove Serial Flash

```

|-----|
| Reserve for BIOS boot function

```

When EECS switch to be D3-Delink sideband signal, Serial Flash function is disabled.

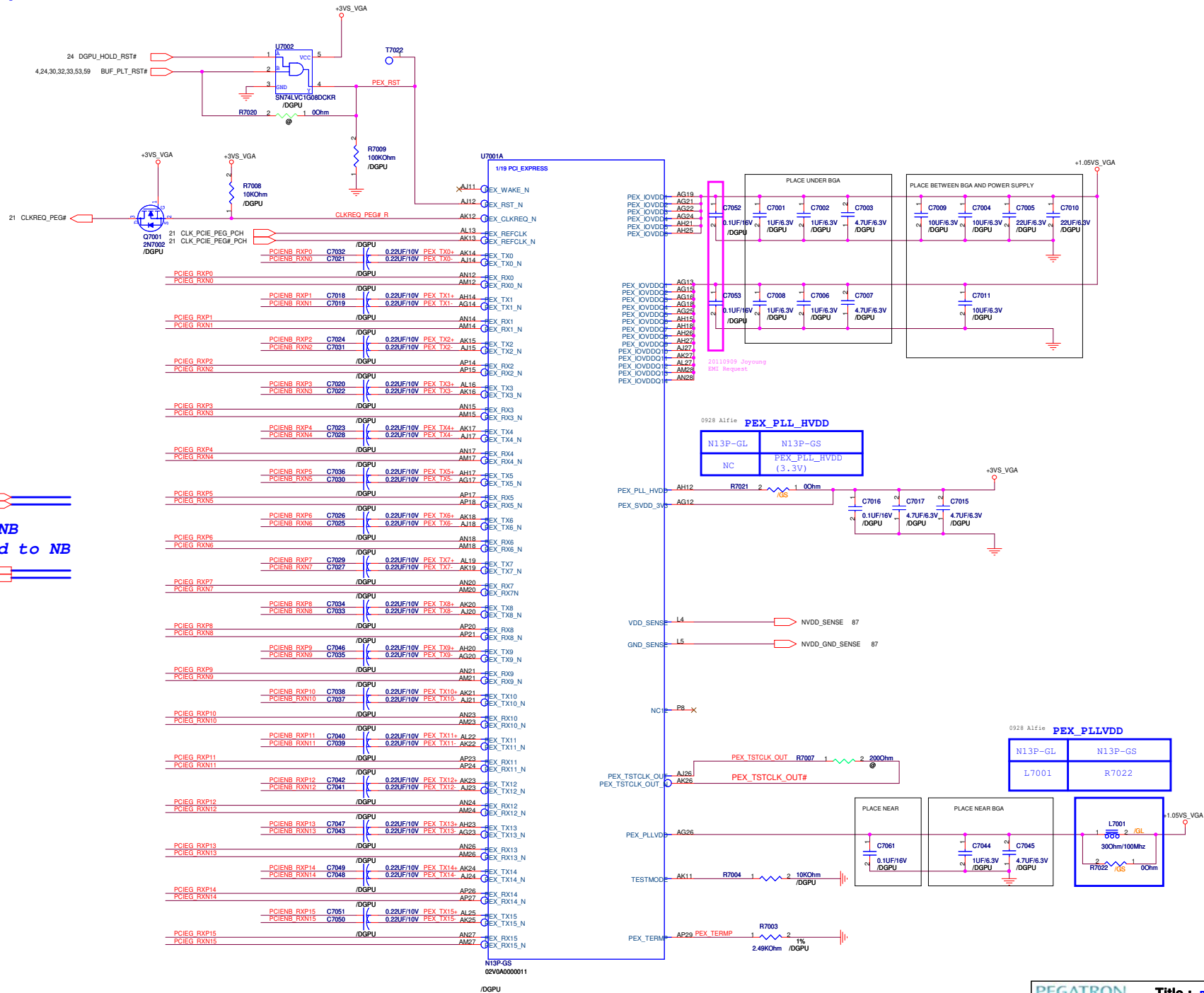
Pin Name	Description
SP1	SD_D7/XD_RDY
SP2	SD_D6/XD_RE#
SP3	SD_D5/XD_CE#
SP4	SD_D4/XD_WE#
SP5	MS_BS/XD_CLE
SP6	MS_D5/XD_ALE
SP7	MS_D1/XD_WP#
SP8	MS_D4/XD_D0
SP9	MS_D0/XD_D1
SP10	MS_D2/XD_D2
SP11	MS_D6/XD_D3
SP12	MS_D3/XD_D4
SP13	MS_D7/XD_D5
SP14	MS_CLK/XD_D6
SP15	SD_WP/XD_D7

PEGATRON Title : **RTS5209**

Engineer: JAY TSAI		
Size C	Project Name MA50	Rev 1.0
Date: Monday, February 13, 2012	Sheet 67 of 93	

PEGATRON		Title : <u>USB_USB Port</u>
<OrgName>		Engineer: <u>Joyoung_Chianhg</u>
Size B	Project Name MA50	Rev 1.3
Date: <u>Monday, February 13, 2012</u>		Sheet <u>69</u> of <u>93</u>

Frank
20110513 Change N13P GPU.



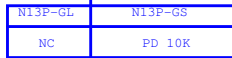
PEX=> From NB
EXP: VGA Card to NB

3 PCIEG_RXP[0..15]
3 PCIEG_RXN[0..15]

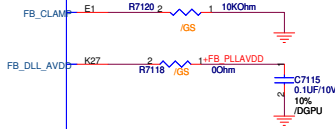
76 FBAD0[0..63]
76 FBA_CMD[0..31]
76 FBADQM[0..7]
76 FBADQS_WP[0..7]
76 FBADQS_RN[0..7]



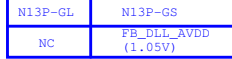
FB_CLAMP



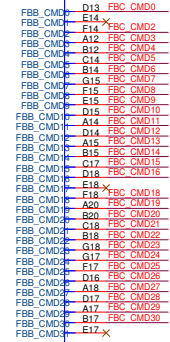
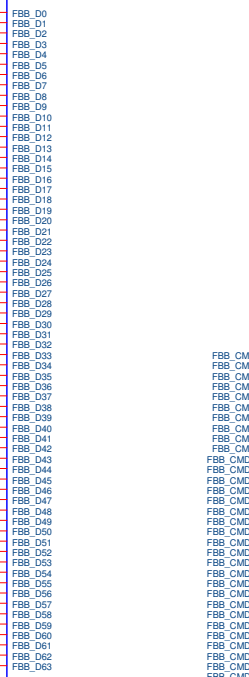
BOT SIDE



FB_DLL_AVDD



77 FBAD0[0..63]
77 FBC_CMD[0..31]
77 FBADQM[0..7]
77 FBADQS_WP[0..7]
77 FBADQS_RN[0..7]



U7001H

1019 XVDD

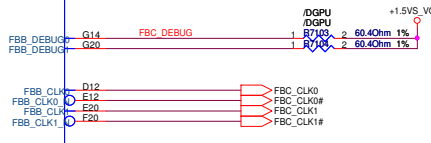
CONFIGURABLE POWER CHANNELS



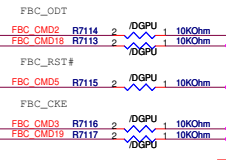
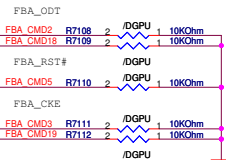
N13P-GS

02V0A0000011

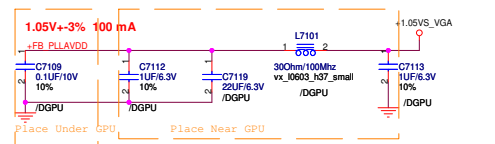
/DGPU



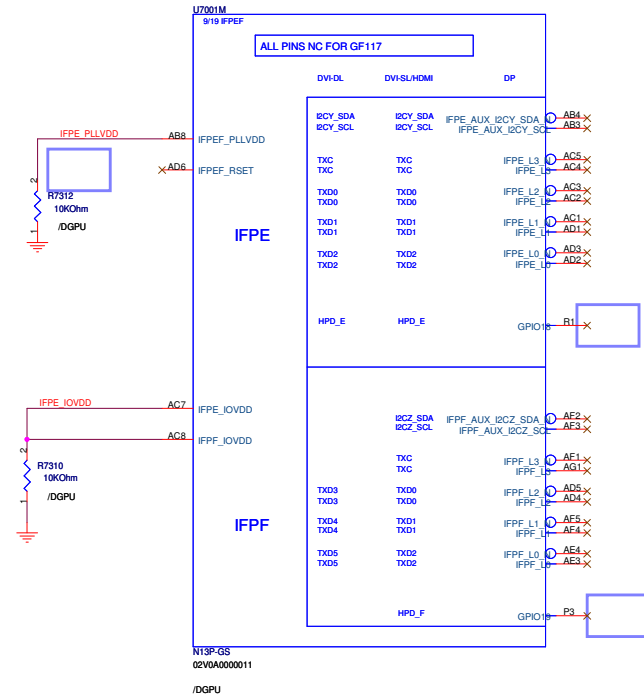
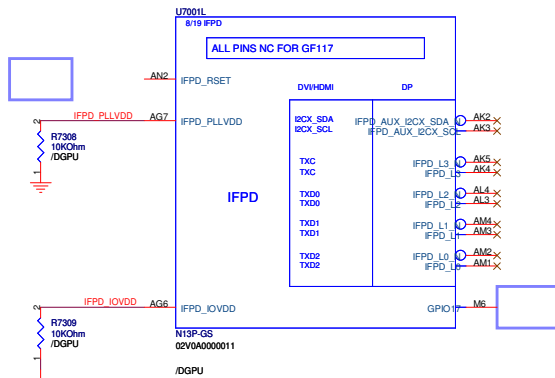
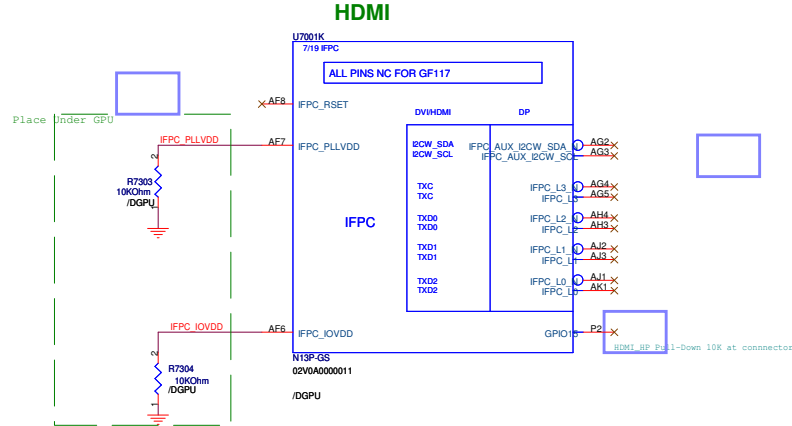
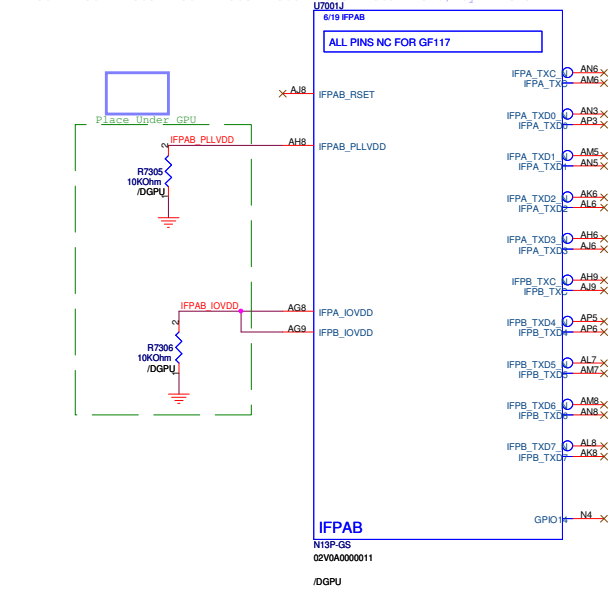
FBB_PLL_AVDD

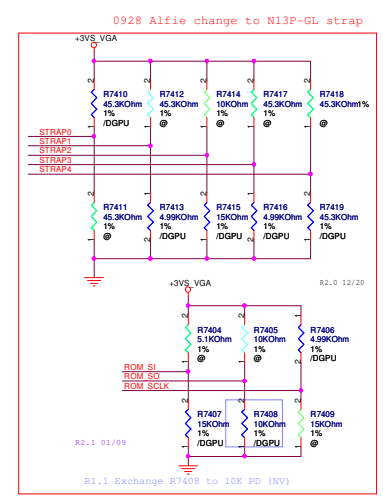
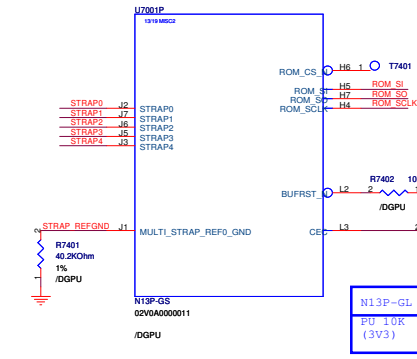


Frank 20110613 Vender suggest C7119 change 22UF.

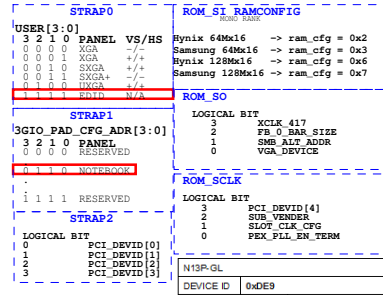


LVDS
R1.1 Remove the TP (T7301 T7311 T7302 T7307 T7303 T7304 T7305 T7306 T7308 T7309 T7310) by Nvidia



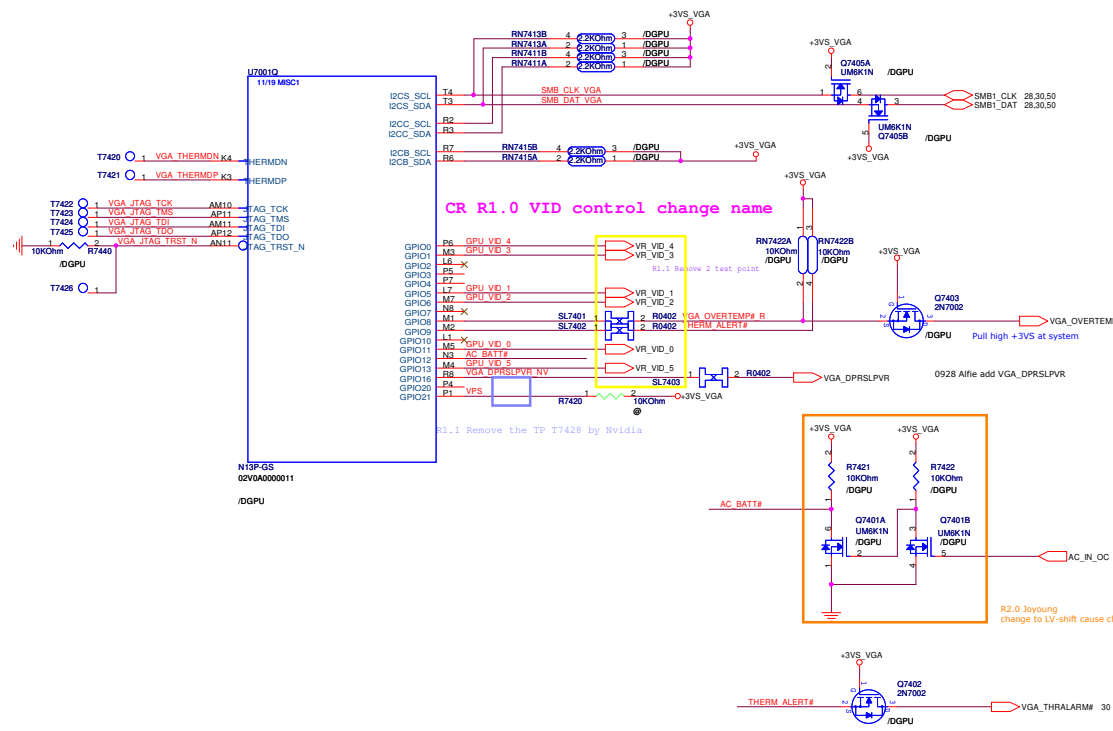


TERMINATION RESISTANCE	TERMINATION VOLTAGE	
	3V3 [3:0]	GND [3:0]
5K	1000 B	0000 0
10K	1001 B	0001 1
15K	1010 A	0010 2
20K	1011 B	0011 3
25K	1100 C	0100 4
30K	1101 D	0101 5
35K	1110 E	0110 6
45K	1111 F	0111 7

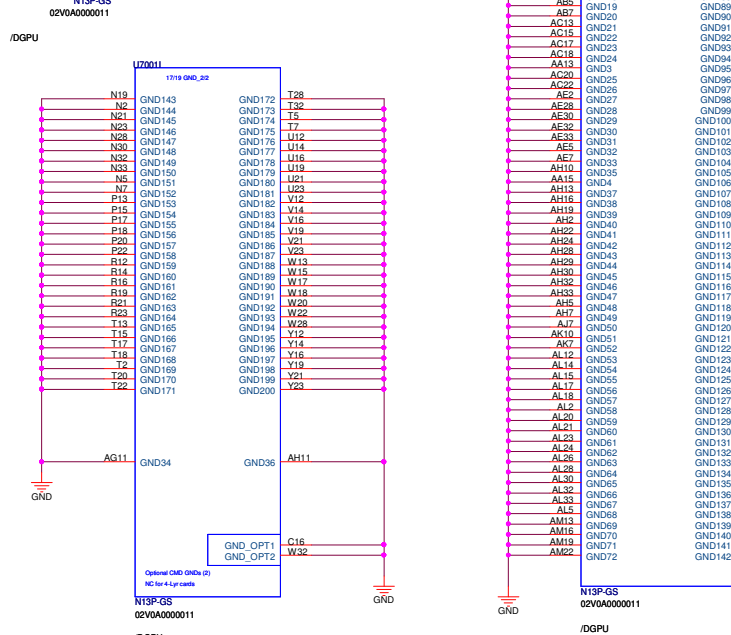


N13P-GL			
DEVICE ID	0x0E9		
STRAP0	45K PU	ROM_SCLK	15K PD
STRAP1	45K PD	ROM_SI	64x16
STRAP2	10K PU		
STRAP3	NC		
STRAP4	NC		
		ROM_SO	30K PD

VRAM need change BOM



R1.1 Remove L_VDDER_VGA & LCD_BKEN_VGA signals, No function request on the pin (NV)



PLACE CLOSE TO GPU BALLS

+1.5VS_VGA

/DGPU 1 2 R7507 40.20ohm

/DGPU 1 2 R7509 42.20ohm

/DGPU 1 2 R7510

51.10ohm

10V220000319

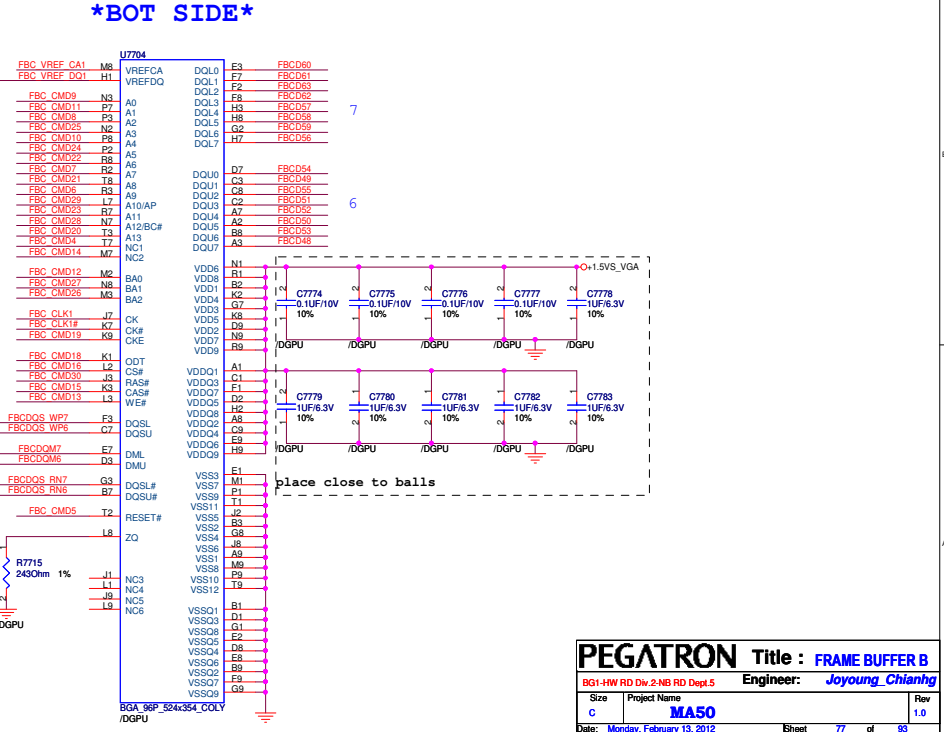
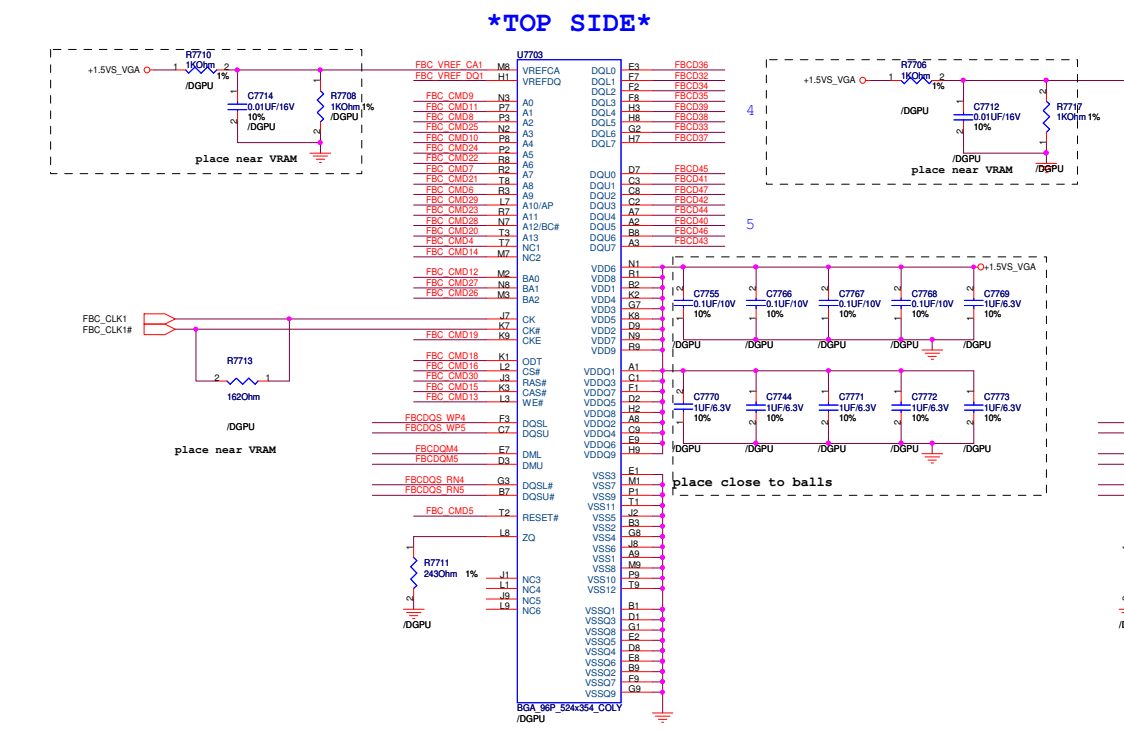
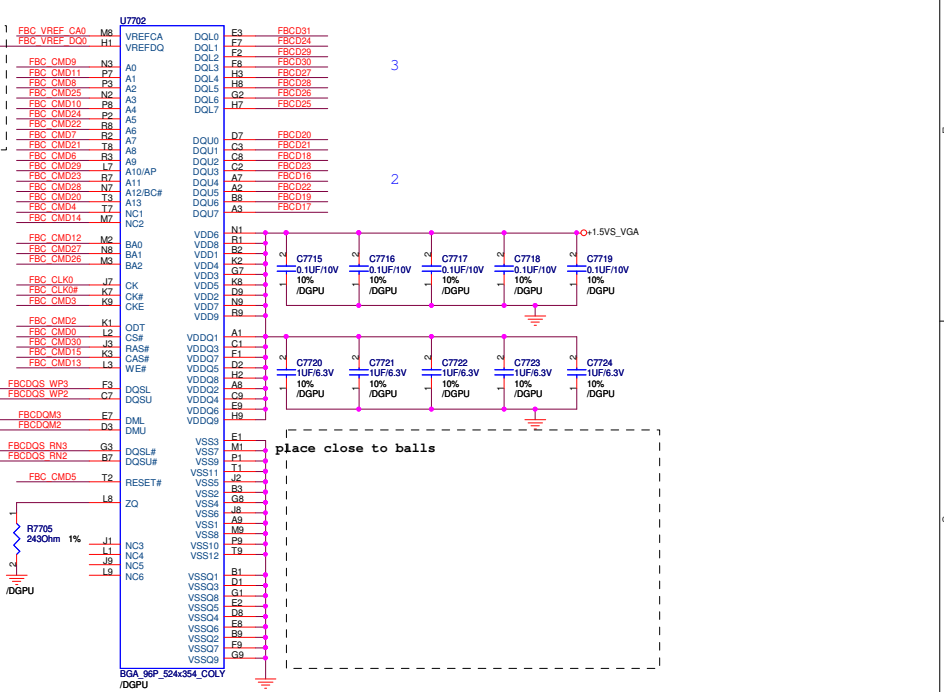
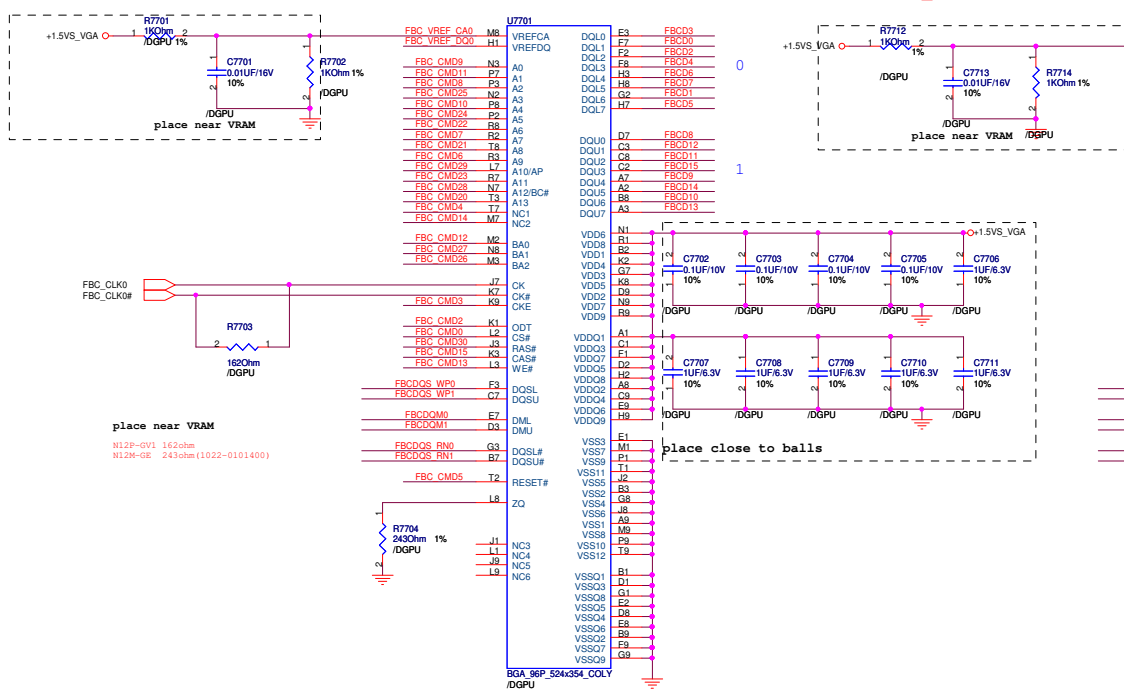
GND

```
Frank
20110613 Follow Vender and spec suggest=>Remove R7509 change 42.2 ohm
Joyoung
20110913 Follow Vendor spec PUN-05893-001_v02=>Change R7510 to 51.1 ohm
```

TOP SIDE



VRAM CH C



	5	4	3	2	1
D					
C					
B					
A					
	5	4	3	2	1

PEGATRON		Title : Connector, LED	
PEGATRON COMPUTER INC		Engineer: Joyoung Chianhg	
Size	Project Name		Rev
C	P/N	MASO <OrgAddr2>	1.0
Date: Monday, February 13, 2012		Sheet	78 of 83

	5	4	3	2	1
D					
C					
B					
A					
	5	4	3	2	1

PEGATRON		Title : GPU PWR/GND	
PEGATRON COMPUTER INC		Engineer: Joyoung Chianhg	
Size	Project Name	Rev	
C	P/N	1.0	
Date: Monday, February 13, 2012		Sheet	79 of 83

Huron River



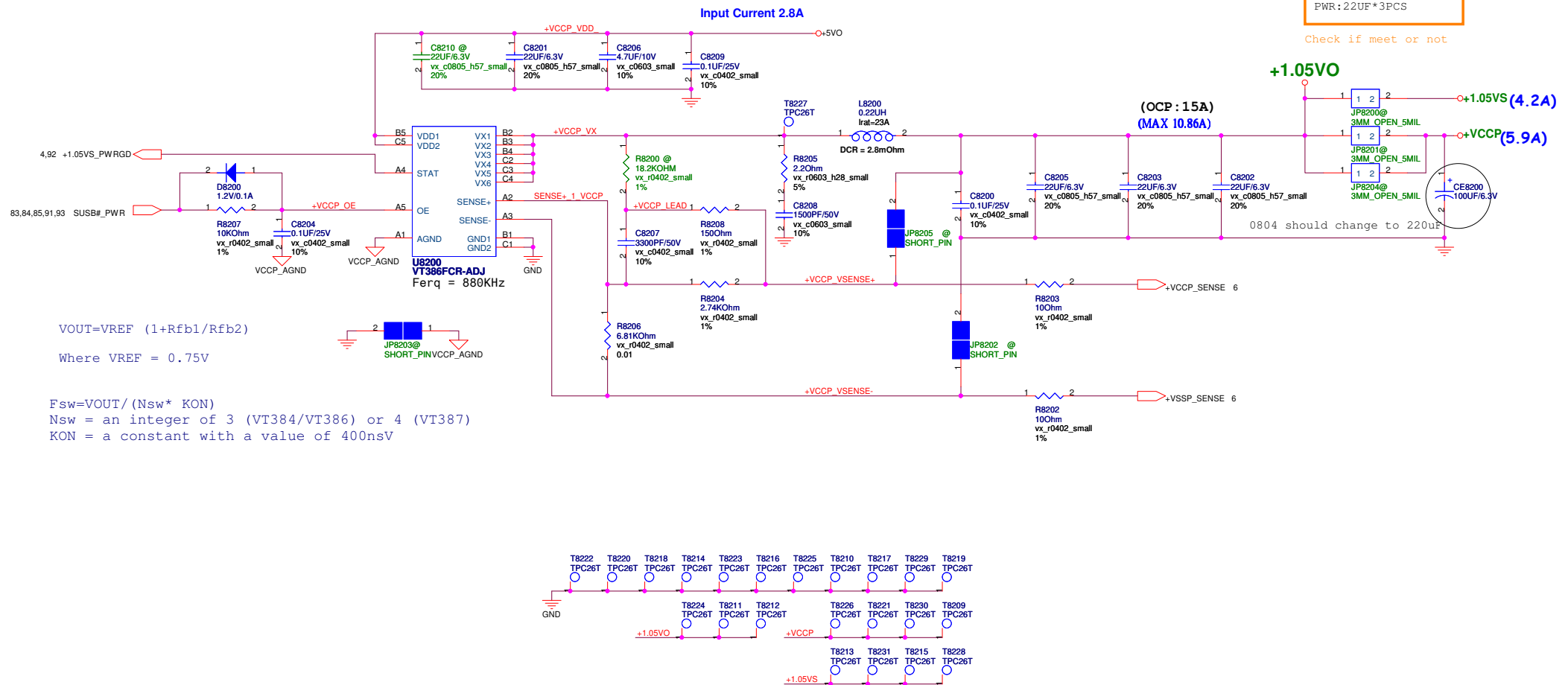
Engineer: **Clark Liang**

MA50
Sheet 80 of 80

Date: Monday, February 13, 2012 8:00 AM of 94

Date: Monday, February 13, 2012 Sheet 81 of 94

+1.05V_O POWER SUPPLY



<Variant Name>

PEGATRON Title : POWER_VCCP

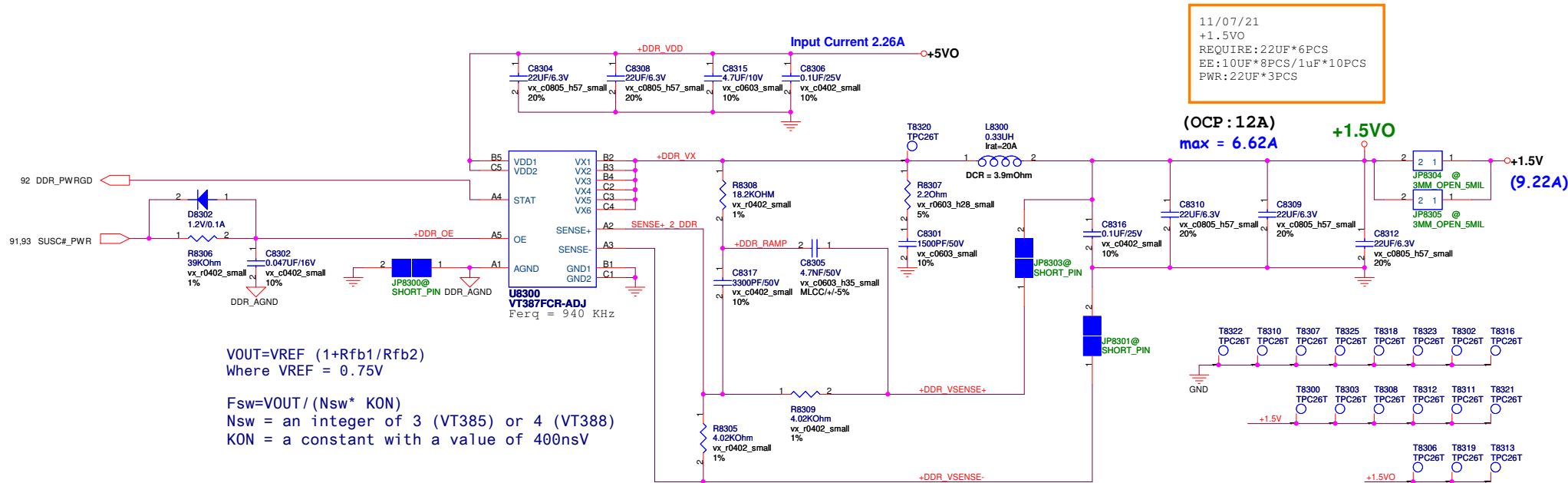
Engineer: **Clark Liang**

Size	Project Name	Re
------	--------------	----

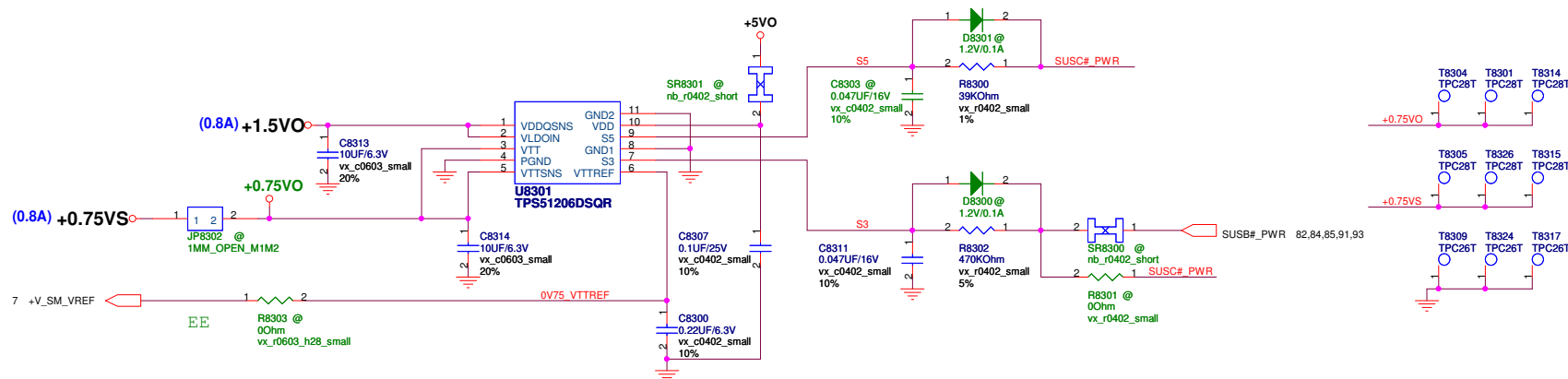
Custom	MA50	1.0
--------	------	-----

Date: Monday, February 13, 2012 Sheet 82 of 94

+1.5VO POWER SUPPLY



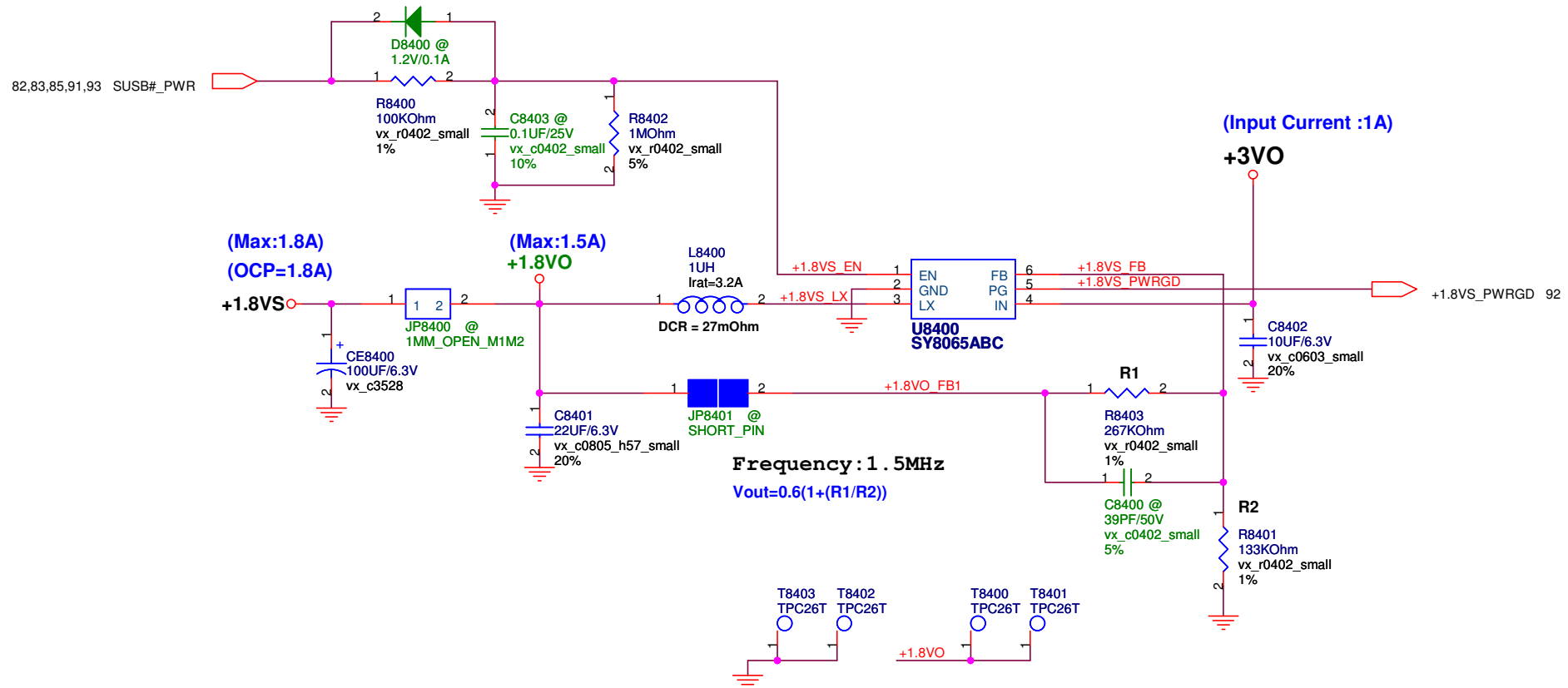
+0.75VS POWER SUPPLY



<Variant Name>

PEGATRON		Title :	POWER_DDR & VTT	
		Engineer:	Clark Liang	
Size Custom	Project Name MA50			Rev 1.0
Date: Monday, February 13, 2012		Sheet	83	of 94

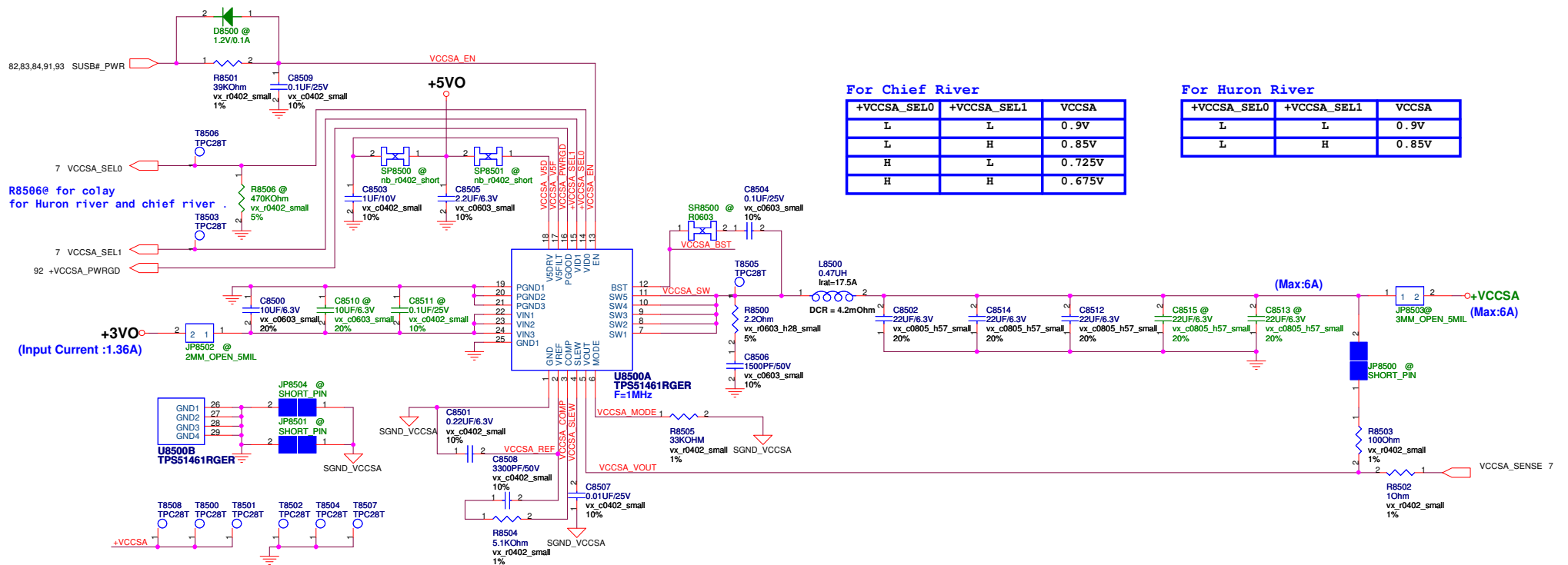
+1.8VS POWER SUPPLY



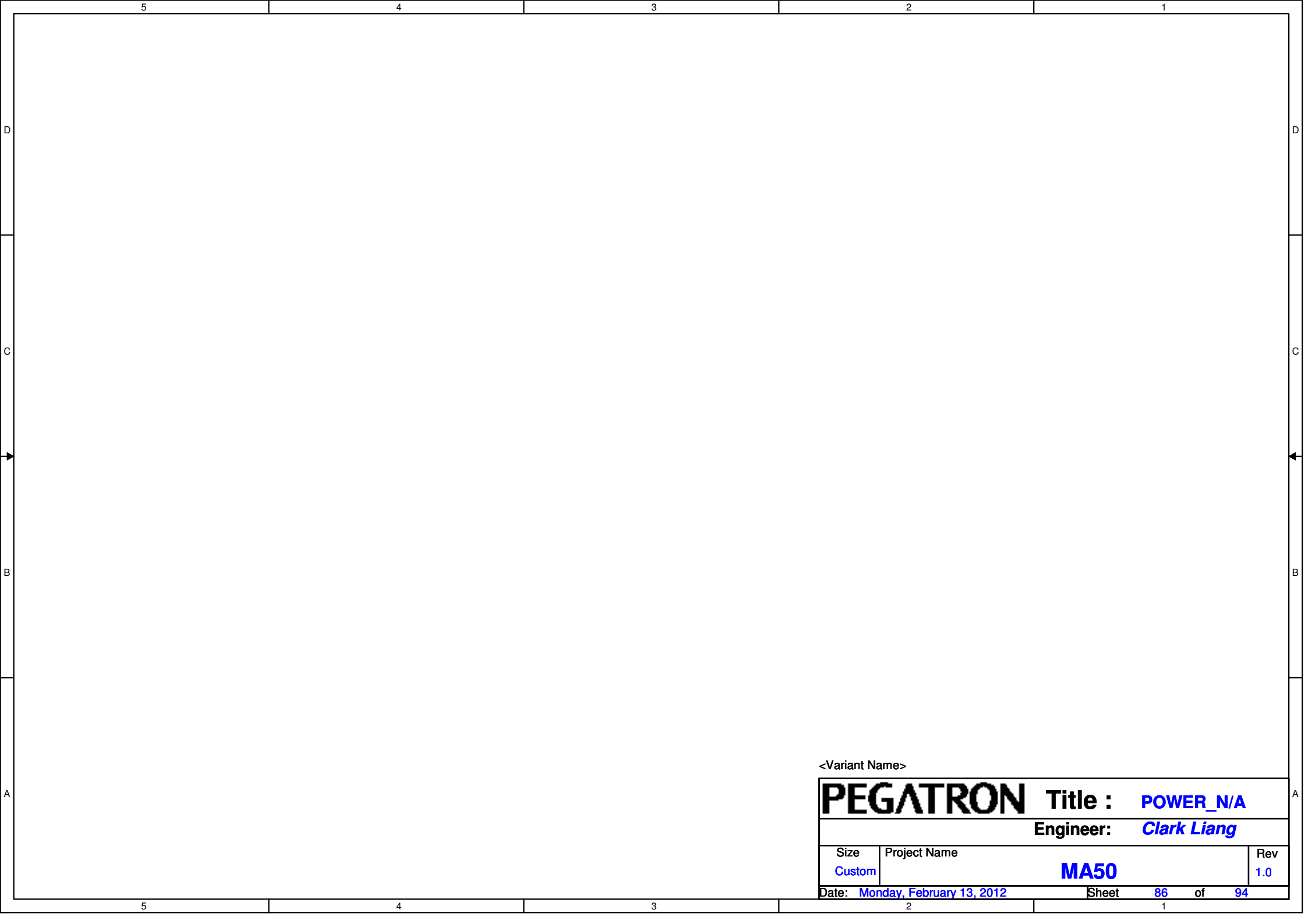
<Variant Name>

PEGATRON		Title :	POWER_+1.8VS
		Engineer:	Clark Liang
Size Custom	Project Name MA50		Rev 1.0
Date: Monday, February 13, 2012		Sheet	84 of 94

IVB VCCSA POWER SUPPLY



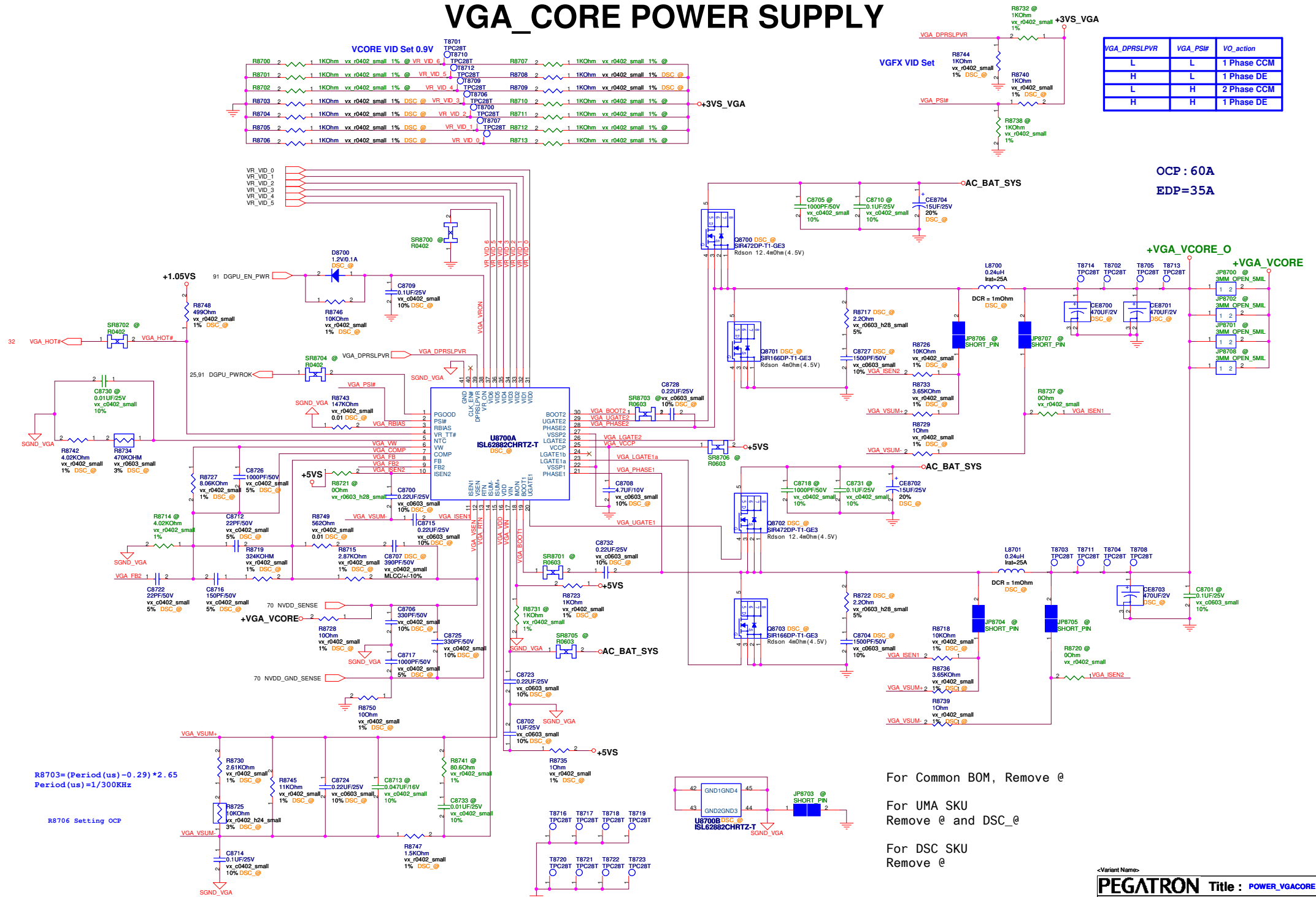
<Variant Name>



<Variant Name>

PEGATRON		Title :	POWER_N/A
		Engineer:	Clark Liang
Size	Project Name		Rev
Custom	MA50		1.0
Date: Monday, February 13, 2012		Sheet	86 of 94

VGA_CORE POWER SUPPLY



For Common BOM, Remove @

For UMA SKU
Remove @ and DSC_@

For DSC SKU
Remove @

<Variant Name>

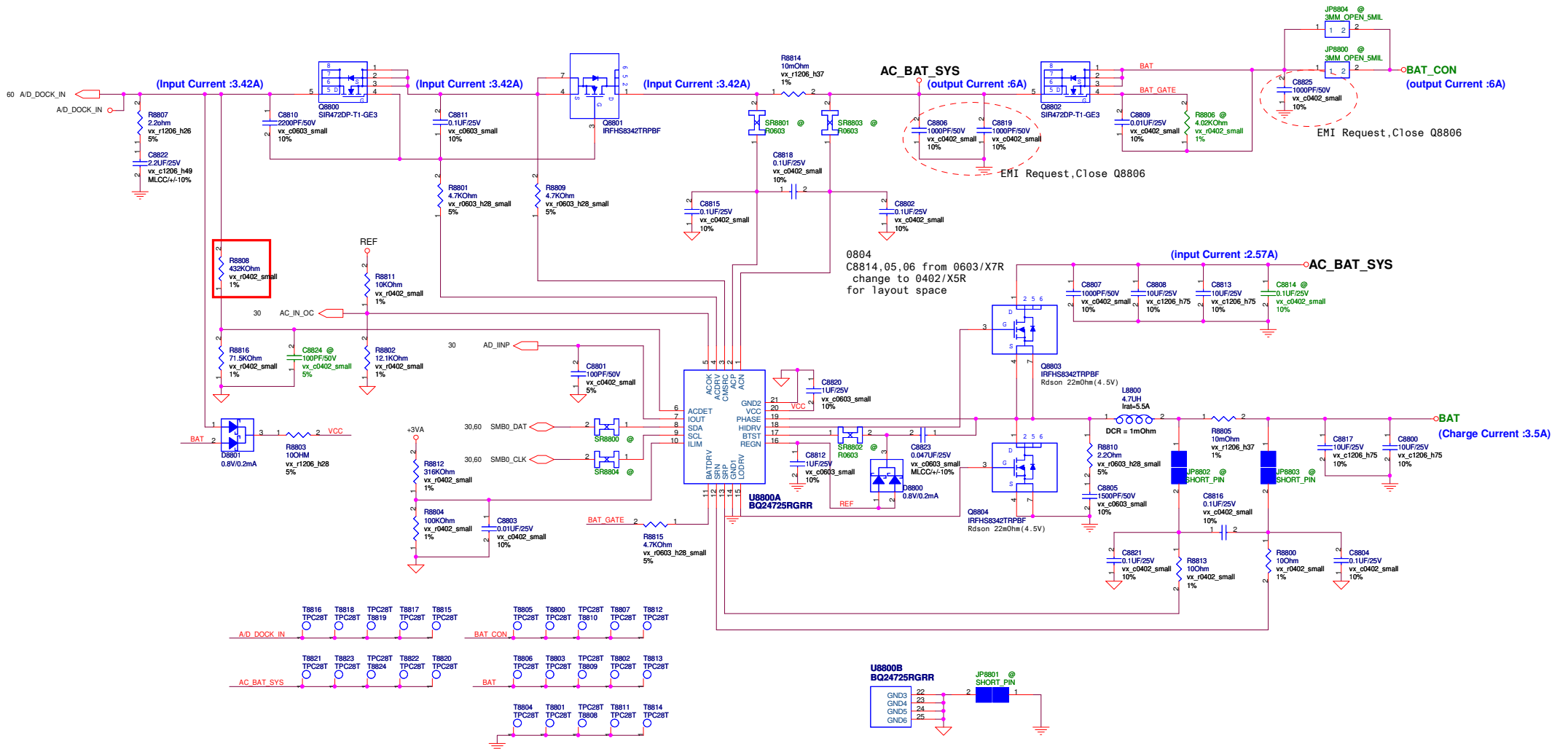
PEGATRON Title : POWER_VGACORE

Engineer: *Clark Liang*

Size	Project Name	Rev
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Custom	MA50	1.0
Date: Monday, February 13, 2012	Sheet 87 of 94	

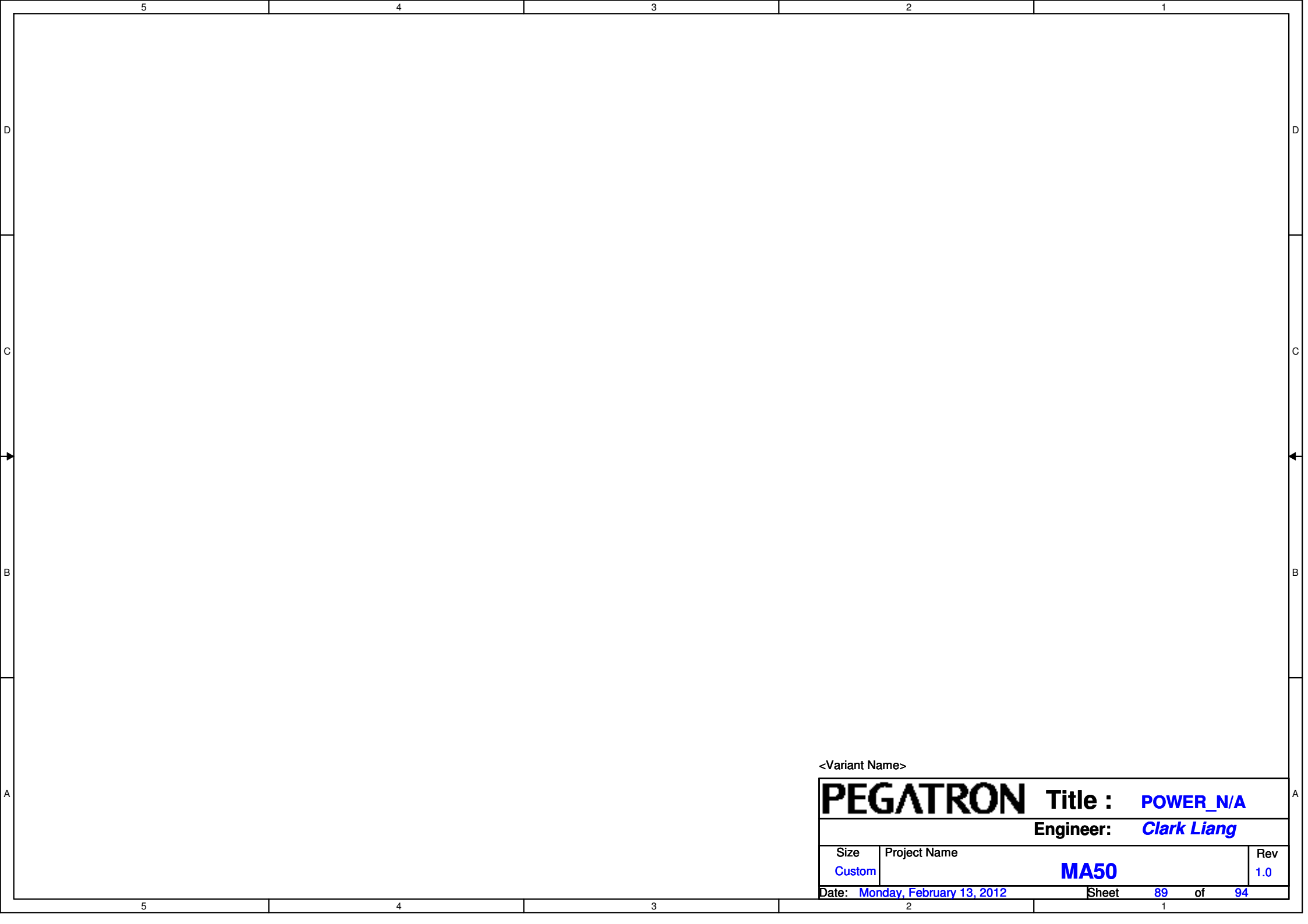
BATTERY CHARGER



<Variant Name>

PEGATRON Title : POWER_CHARGER

Engineer: Clark Liang					
Size	Project Name				Rev
Custom	MA50				1.0
Date: Monday, February 13, 2012			Sheet 88 of 94		



<Variant Name>

PEGATRON		Title :	POWER_N/A
		Engineer:	Clark Liang
Size	Project Name		Rev
Custom	MA50		1.0
Date: Monday, February 13, 2012		Sheet	89 of 94

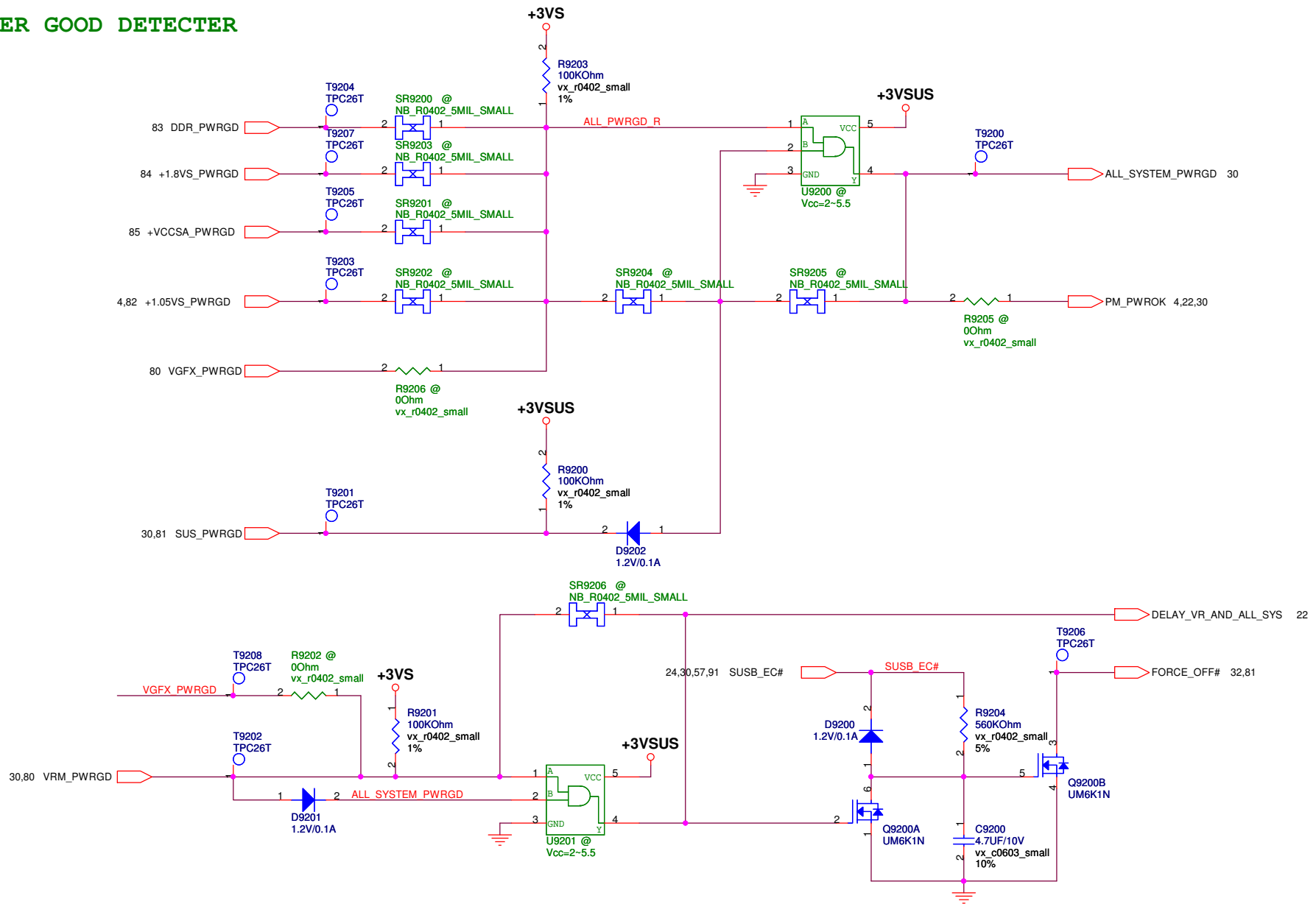
BATTERY IN DETECT



<Variant Name>

PEGATRON		Title : POWER_DETECT	
		Engineer: Clark Liang	
Size Custom	Project Name MA50		Rev 1.0
Date: Monday, February 13, 2012		Sheet	90 of 94

POWER GOOD DETECTOR

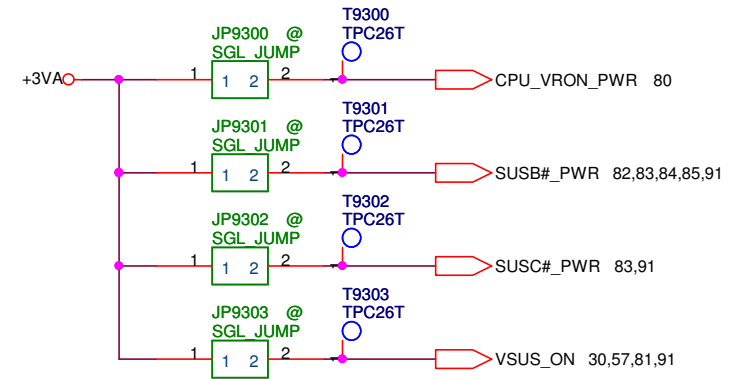


<Variant Name>

PEGATRON		Title : POWER_PROTECT	
Size		Engineer: Clark Liang	
Custom	Project Name	MA50	
Date: Monday, February 13, 2012	Sheet	92	of 94
Rev		1.0	

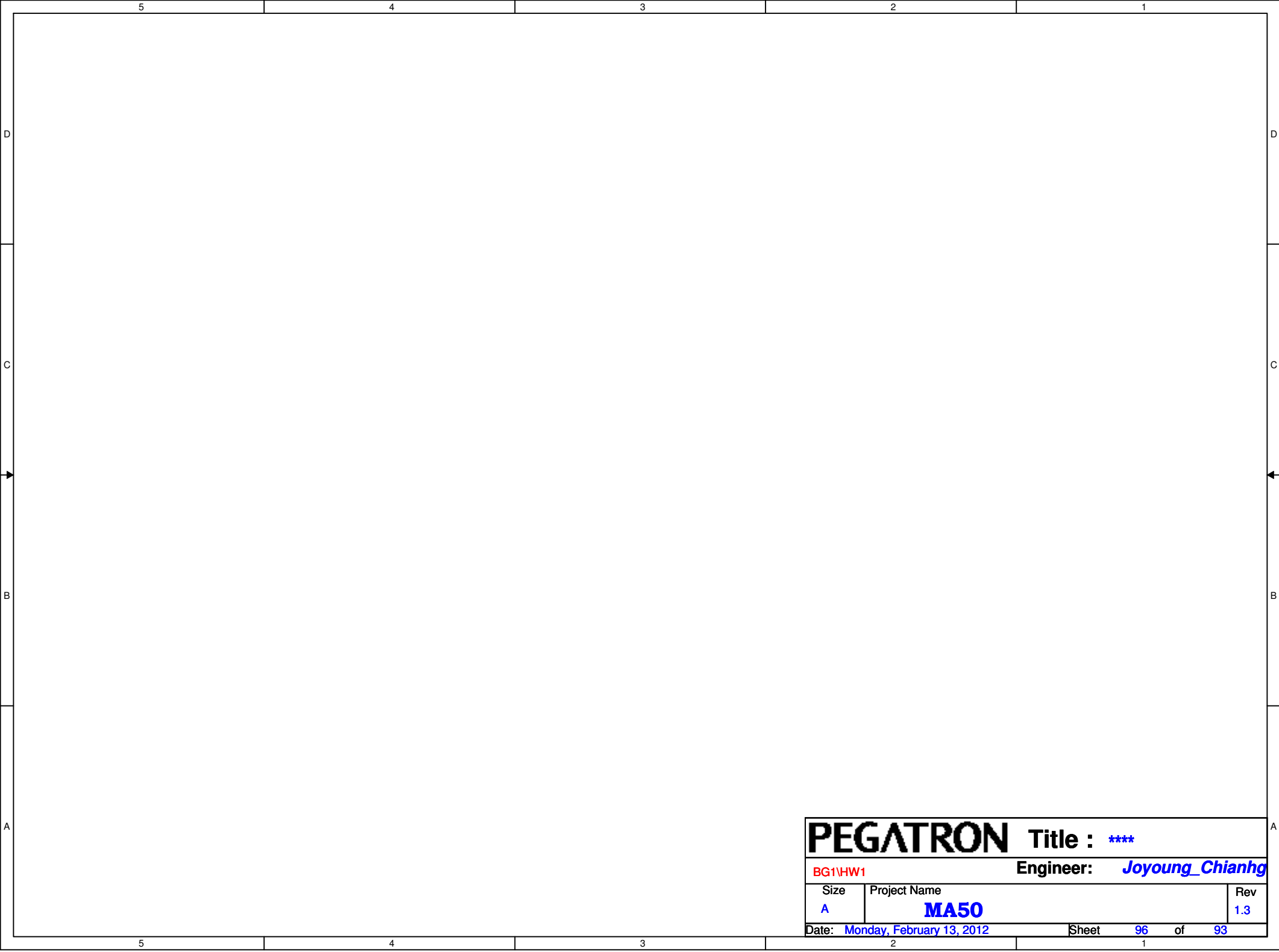
AC_BAT_SYS	AC_BAT_SYS	45,53,81,87,88
BAT	BAT	88
BAT_CON	BAT_CON	60,88
+5VA	+5VA	37,60,81,91
+3VA	+3VA	6,20,26,27,30,31,57,59,60,81,88
+5VO	+5VO	52,65,80,81,82,83,85,91
+3VO	+3VO	53,81,84,85,91
+1.8VO	+1.8VO	60,84
+1.5VO	+1.5VO	83,91
+1.05VO	+1.05VO	82,91
+0.75VO	+0.75VO	83
+12VSUS	+12VSUS	28,51,81,91
+5VSUS	+5VSUS	51,57,59,91
+3VSUS	+3VSUS	4,22,24,28,30,60,81,92
+12V	+12V	60,91
+5V	+5V	57,59,60,91
+3V	+3V	24,45,57,59,61,91
+1.5V	+1.5V	5,16,17,18,57,60,83
+12VS	+12VS	28,36,48,91
+5VS	+5VS	27,36,37,48,50,51,57,80,87,91
+3VS	+3VS	17,20,21,22,23,24,25,26,27,28,30,32,33,36,37,44,45,48,50,51,53,57,59,61,80,91,92
+1.8VS	+1.8VS	7,25,26,57,80,84
+1.5VS	+1.5VS	7,26,53,57,91
+1.05VS	+1.05VS	26,27,57,82,87
+VCCSA	+VCCSA	7,85
+0.75VS	+0.75VS	16,17,57,83
+VCORE	+VCORE	6,9,11,80
+VGFX_CORE	+VGFX_CORE	7,9,80
+12VS_VGA	+12VS_VGA	60,91
+3VS_VGA	+3VS_VGA	57,70,72,74,75,87,91
+1.5VS_VGA	+1.5VS_VGA	57,71,75,76,77,91
+1.05VS_VGA	+1.05VS_VGA	57,70,71,72,91

FOR POWER TEST



<Variant Name>

PEGATRON		Title : POWER_SIGNAL	
		Engineer: Clark Liang	
Size	Project Name		Rev
Custom	MA50		1.0
Date: Monday, February 13, 2012		Sheet	93 of 94



PEGATRON			Title : ****		
BG1\HW1			Engineer: Joyoung_Chianhg		
Size	Project Name				Rev
A	MA50				1.3
Date: Monday, February 13, 2012			Sheet	96	of 93

SR BOM change

- SR1.1 Un-mount Q5602, Q5601 and mount R5323 and R5310
- SR1.2 CE5001 un-mount
- SR1.3 L3602 mount
- SR1.4 R7005 un-mount
- SR1.5 R7410 change 10K ohm
- SR1.6 R4504 change 10K ohm for LVDS backlight
- SR1.7 R7430, R7432, R7433 un-mount
- SR1.8 R7608, R7611 change 162 ohm

ER

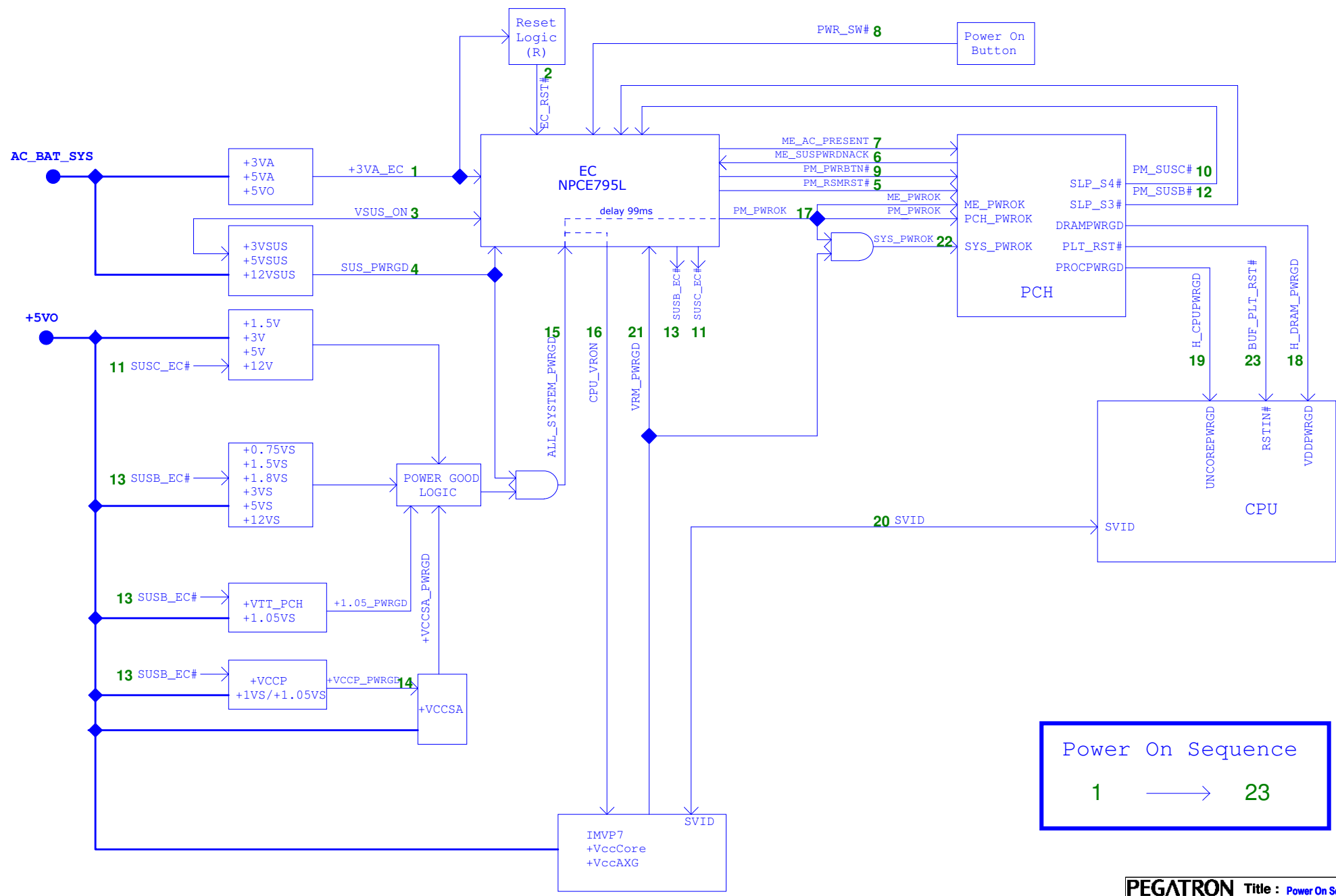
- ER1.1 PI pin connect to ESD and VDD pin reserve 0.1 uF cap
- ER1.2 Add diode and reserve 0 ohm for AC adapter plug in /out voice
- ER1.3 U5201 change G547G1P81U for Desing IP
- ER1.4 Add Card Reader LED
- ER1.5 J3701, J3702, J4601, J5201, J5304,J5001 chang connector
- ER1.6 R6505~R6508 change 0603 size
- ER1.7 D4801 contact to 2.2K ohm for EA solution in HDMI issue
- ER1.8 CPU_THERM# contact to FORCE_OFF#
- ER1.9 RTC battery connector (J2001)Pin1, Pin2 swap
- ER1.10 D3707, D4618, D5201, D5301, D6502, D6503, D6802 VDD pin reserve 0.1 uF cap
- ER1.11 R3720 R3721 change 51ohm for consumer spec in HP
- ER1.12 L4601, L4602, L4603 change 27nH and add C4622, C4623, C4624 for EA solution in CRT
- ER1.13 L5301, L5302, L5306 change 0 ohm and L5305 change short pin, C5321, C5327,C5307, C5322, C5315, C5305, C5313 change umount
- ER1.14 Change R4566 from 300(0603) to 150(0402) for LVDS power sequence solution
- ER1.15 USB port 0 and port 1 swap
- ER1.16 Vcore_add CE8002&CE8006 to replace CE0601&CE0602
- ER1.17 VGFX_CORE(IGPU) add CE8007 to replace CE0705
- ER1.18 reserve M_VREF schematic
- ER1.19 Reserve C2623, C2624, C4514, C4515 for WLAN solution
- ER1.20 Reserve C4510, C4512, C4513 for 3G and L6002~L6004, L4502 change 47 ohm Bead
- ER1.21 C6007, C6006 mount for WLAN
- ER1.22 RN3002 change 2R4P
- ER1.23 LED and BT schematic change to LED board
- ER1.24 LED power change 5VSUS, so R5618, R5616, R5623 change 560 ohm
- ER1.25 VRAM change co-lay footprint
- ER1.26 Reserve C5601, C5602, C5603, C6356, C6357 to 47pF for RF request
- ER1.27 Reserve C4516, C4517 to 10pF for RF request
- ER1.28 U6504,U6505 change AZ3028 for EMI request
- ER1.29 D6401, D6501, D6502 change ESD AZ5023 in for EMI request in LAN function
- ER1.30 Add C6010 C6011 for EMI request
- ER1.31 Merge Q6704 and remove U6704
- ER1.32 D3720 change to mount for EMI request
- ER1.34 Reserve C6913(47PF), C6902(0.1uF), C6623(47PF), C6606(22uF) for 3G
- ER1.35 L6601=>0901-00HI000 FERRITE BEAD(1206)390 OHM/2A

PR

- PR2.1 RTC pin define swap

- PR_S01:Change C3627,C3626 from X5R to Y5V
- PR_S02:According with INTEL datasheet suggest.(Power circuit mount)
- PR_S03:To prevent 誤動作 PCIE Wake.
- PR_S04:To change WLAN LED control by MODULE then gate control by 3G LED.
- PR_S05:To change 3G LED control by MODULE.
- PR_S06:To prevent leakage current and mount R for cost down.
- PR_S07:RF reserve.
- PR_S08:Move P.U 10K near 3G connector.
- PR_S09:Change LED POWER rail from +5VSUS_LEDDDB(+5VSUS) to +5VA_LEDDDB(+5VA) .(To resolve Battery LL issue)
- PR_S10:Change LED POWER rail from +5VSUS_LEDDDB(+5VSUS) to +5V_LEDDDB(+5V)
- PR_S11:Del JP, +3VS_CR change Net name to +3VS
- PR_S12:ESD change solution ,Add U6512 ,Del C6509,D6501~3,U6502,U6503,D6401
- PR_S13:Change NET name to +3VS
- PR_S14:Change 10uF to 22uF for wave of CRT display.
- PR_S15:Add 10uF (C6803)for USB droop test.
- PR_S16:D5201 PIN Swap
- PR_S17:ME modify.(H6532,8,1,9,4,3,5,H6945),DEL H6944
- PR_S18:EMI add.
- PR_S19:Change to unmount for ME
- PR_S20:RF request.
- PR_S21:LED light fine-tune.
- PR_S22:BIOS request for UMA and DSC platform identifying.

Power On Sequence Diagram G3-S0 R0.3 (non-iAMT, non-Deep Sx)



Power On Sequence

1 → 23

Power On Sequence Diagram G3-S0 R0.3 (non-iAMT, non-Deep Sx)

